

FTLX3671MTCXX

Industrial Temperature DWDM 10G Multi-Rate, 40km SFP+ Transceiver

FTLX3671MTCxx transceivers are Enhanced Small Form Factor Pluggable SFP+ transceivers designed for use in DWDM links up to 40km of G.652 single mode fiber, for multi-rate applications from 1.2 through 11.3 Gb/s, carrying 1-10G Ethernet, 1-10G Fibre Channel, 10G OTN traffic or CPRI options 2 through 8 traffic. The FTLX3671MTCxx transceivers are compliant with SFF-8431¹ and SFF-8432². FinisarFTLX3671MTCxx transceivers use internal re-timers (clock and data recovery or CDR) for the transmitter and the receiver to guarantee compliance with the SONET/SDH jitter requirements. Digital diagnostics functions are available via a 2-wire serial interface, as specified in SFF-84723. FinisarFTLX3671MTCxx transceivers are RoHS compliant per Directive 2011/65/EU 4,5.



FEATURES

- 100 GHz spacing, DWDM C-band
- Up to 40km link length
- PIN Receiver with limiting interface
- 1.2 through 11.3 Gb/s data rates
- -40/85°C case temperature range
- Single 3.3V power supply
- Cooled 1550nm EML laser
- Hot-pluggable SFP+ footprint
- Duplex LC connector
- Built-in digital diagnostic functions
- RoHS-6 compliant

APPLICATIONS

- DWDM 40km links for:
- Fibre Channel 2G through 10G
- Ethernet 1G through 10G
- CPRI options 2 through 8
- OTN OTU 1, 2 and 2f

Product Selection

FTLX3671MTCxx

xx=ITU-T Grid Channel (see next page)

Product Ordering Codes / Channel Selection

Channel	Product Code	Frequency (THz)	Center Wave-length (nm)
C20	FTLX3671MTC20	192.00	1561.42
C21	FTLX3671MTC21	192.10	1560.61
C22	FTLX3671MTC22	192.20	1559.79
C23	FTLX3671MTC23	192.30	1558.98
C24	FTLX3671MTC24	192.40	1558.17
C25	FTLX3671MTC25	192.50	1557.36
C26	FTLX3671MTC26	192.60	1556.55
C27	FTLX3671MTC27	192.70	1555.75
C28	FTLX3671MTC28	192.80	1554.94
C29	FTLX3671MTC29	192.90	1554.13
C30	FTLX3671MTC30	193.00	1553.33
C31	FTLX3671MTC31	193.10	1552.52
C32	FTLX3671MTC32	193.20	1551.72
C33	FTLX3671MTC33	193.30	1550.92
C34	FTLX3671MTC34	193.40	1550.12
C35	FTLX3671MTC35	193.50	1549.32
C36	FTLX3671MTC36	193.60	1548.51
C37	FTLX3671MTC37	193.70	1547.72
C38	FTLX3671MTC38	193.80	1546.92
C39	FTLX3671MTC39	193.90	1546.12
C40	FTLX3671MTC40	194.00	1545.32

Channel	Product Code	Frequency (THz)	Center Wave-length (nm)
C41	FTLX3671MTC41	194.10	1544.53
C42	FTLX3671MTC42	194.20	1543.73
C43	FTLX3671MTC43	194.30	1542.94
C44	FTLX3671MTC44	194.40	1542.14
C45	FTLX3671MTC45	194.50	1541.35
C46	FTLX3671MTC46	194.60	1540.56
C47	FTLX3671MTC47	194.70	1539.77
C48	FTLX3671MTC48	194.80	1538.98
C49	FTLX3671MTC49	194.90	1538.19
C50	FTLX3671MTC50	195.00	1537.40
C51	FTLX3671MTC51	195.10	1536.61
C52	FTLX3671MTC52	195.20	1535.82
C53	FTLX3671MTC53	195.30	1535.04
C54	FTLX3671MTC54	195.40	1534.25
C55	FTLX3671MTC55	195.50	1533.47
C56	FTLX3671MTC56	195.60	1532.68
C57	FTLX3671MTC57	195.70	1531.90
C58	FTLX3671MTC58	195.80	1531.12
C59	FTLX3671MTC59	195.90	1530.33
C60	FTLX3671MTC60	196.00	1529.55

Table 1. Product ordering codes: the central wavelength is defined as per ITU-T 694.1

I. Pin Descriptions

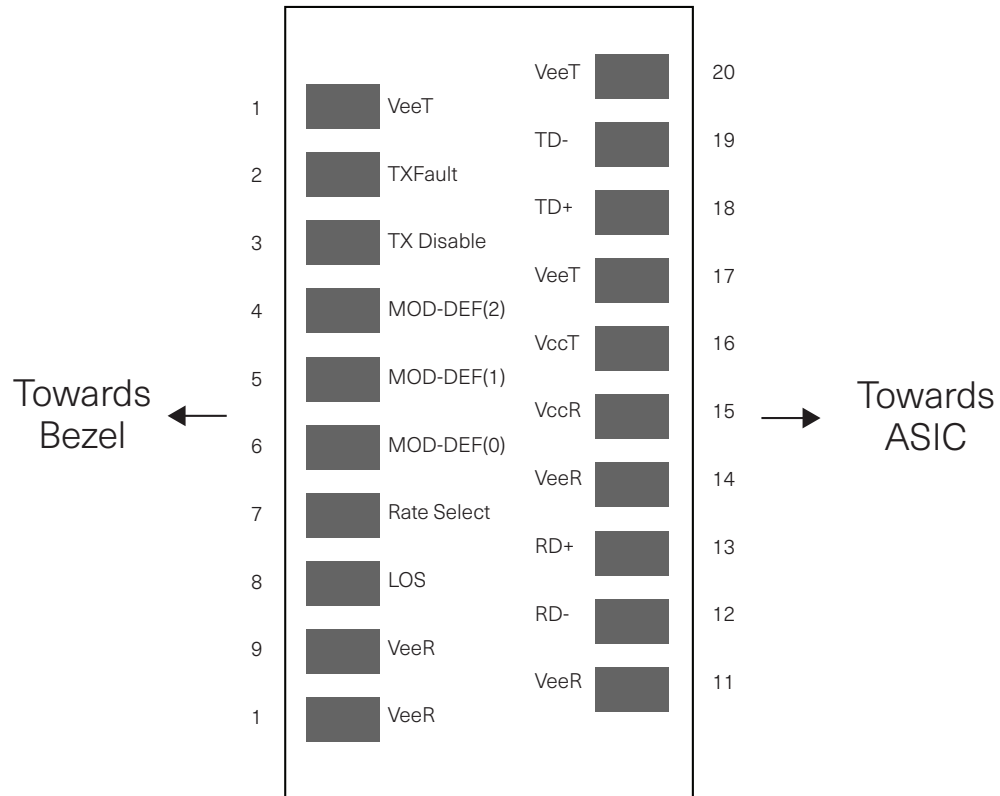


Diagram of Host Board Connector Block Pin Numbers and Names

Pin	Symbol	Name/Description	Notes
1	V _{EET}	Transmitter Ground	1
2	T _{FAULT}	Transmitter Fault	2,3
3	T _{DIS}	Transmitter Disable. Laser output disabled on high or open.	4
4	SDA	2-wire Serial Interface Data Line	2
5	SCL	2-wire Serial Interface Clock Line	2
6	MOD_ABS	Module Absent. Grounded within the module	5
7	RS0	Rate Select 0. Not used.	5
8	RX_LOS	Loss of Signal indication. Logic 0 indicates normal operation.	6
9	RS1	Rate Select 1. Not used.	
10	V _{EER}	Receiver Ground	1
11	V _{EER}	Receiver Ground	1
12	RD-	Receiver Inverted DATA out. AC Coupled.	
13	RD+	Receiver Non-inverted DATA out. AC Coupled.	
14	V _{EER}	Receiver Ground	1
15	V _{CCR}	Receiver Power Supply	7
16	V _{CCT}	Transmitter Power Supply	7
17	V _{EET}	Transmitter Ground	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	
19	TD-	Transmitter Inverted DATA in. AC Coupled.	
20	V _{EET}	Transmitter Ground	1

Notes

1. Circuit ground is internally isolated from chassis ground.
2. Open collector/drain output, which should be pulled up with a 4.7k – 10k Ohms resistor on the host board if intended for use. Pull up voltage should be between 2.0V to Vcc + 0.3V.
3. A high output indicates a transmitter fault caused by either the TX bias current or the TX output power exceeding the preset alarm thresholds. A low output indicates normal operation. In the low state, the output is pulled to <0.8V.
4. Laser output disabled on T_{DIS} >2.0V or open, enabled on T_{DIS} <0.8V.
5. Internally pulled down per SFF-8431 Rev 4.1.
6. LOS is open collector output. Should be pulled up with 4.7k – 10kΩ on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.
7. Internally connected

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	V _{cc}	-0.5		4.0	V	
Storage Temperature	T _s	-40		85	°C	
Case Operating Temperature	RH	0		85	%	1
Relative Humidity	RxDamage	5			dBm	

Notes:

1. Non-condensing

III. Electrical Characteristics (T_{OP} = -40 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	V _{cc}	3.14		3.46		
Transmitter						
Input differential impedance	R _{in}	80	100	120	Ω	
Differential data input swing	V _{in,pp}	120		850	mV	1
Transmit Disable Voltage	V _D	2		V _{cc}	V	
Transmit Enable Voltage	V _{EN}	V _{ee}		V _{ee} + 0.8	V	
Receiver						
Output differential impedance	R _{out}	80	100	120	Ω	
Differential data output swing	V _{out,pp}	300		850	mV	1
Output rise time and fall time	T _r , T _f	24			ps	2
LOS asserted	V _{LOS_A}	V _{cc} -0.8		V _{cc}	V	3
LOS de-asserted	V _{LOS_D}	V _{ee}		V _{ee} + 0.8	V	3
Power Supply Noise Tolerance	V _{ccT} /V _{ccR}	Per SFF-8431 Rev 4.1			mV _{pp}	4
Power Consumption	CDR ON	P _{cons}		1.9	W	5,6
	CDR OFF			1.6	W	6,7

Notes:

1. Internally AC coupled. Data pins connect directly to the CDR.
2. 20 – 80%. Measured with Module Compliance Test Board and OMA test pattern. Use of four 1's and four 0's sequence in the PRBS 9 is an acceptable alternative. SFF-8431 Rev 4.1. Lower limit as per XFP MSA, Tab. 18 (as the SFP+ MSA does not define electrical specifications for transceivers with internal retrimers or CDRs).
3. LOS is an open collector output. Should be pulled up with 4.7kΩ – 10kΩ on the host board. Normal operation is logic 0; loss of signal is logic 1.
4. See Section 2.8.3 of SFF-8431 Rev 4.1.
5. Power consumption measured at 85°C case temperature, beginning of life and 3.3V supply voltage.
6. Contact Finisar if a lower power consumption variant is required.
7. With both receiver and transmitter CDR OFF.

IV. Optical Characteristics ($T_{OP} = -40$ to $85\text{ }^{\circ}\text{C}$, $V_{CC} = 3.14$ to 3.46 Volts)

Parameter			Symbol	Min	Typ	Max	Unit	Ref.
Transmitter								
Average Launch Power			P_{AVE}	1		+4	dBm	
Optical Wavelength			λ_C	As per ITU-T 694.1			dBm	1
Center Wavelength (End of Life)			$\lambda_{C\text{EOL}}$	$\lambda_C \pm 100\text{pm}$			nm	
Side-Mode Suppression Ratio			SMSR	30			dB	
Optical Extinction Ratio			ER	8.2			dB	
Tx Jitter 20kHz - 80MHz			T_{xj1}			0.3	UI	
Tx Jitter 4MHz - 80MHz			T_{xj2}			0.1	UI	2
Average Launch power when Tx is OFF			P_{OFF}			-30	dBm	
Relative Intensity Noise			RIN			-128	dB/Hz	
Receiver								
Optical Center Wavelength			λ_C	1260		1600	nm	
Reflectance			R_{rx}			-27	dB	
Sensitivity (0ps/nm)	Bit Rate (Gb/s)	BER						
	1.2÷10.7	$<10^{-12}$	R_{SENS1}			-16.0	dBm	3,4
	11.1÷11.3	$<10^{-6}$	R_{SENS3}			-15.0		3,5
Sensitivity (800ps/nm)	1.2÷10.7	$<10^{-12}$	R_{SENS4}			-15.0	dBm	3,4,5
	11.1÷11.3	$<10^{-6}$	R_{SENS6}			-14.0		3,5
Overload	<9.83		P_{OVER1}	-1			dBm	6
	≥ 9.83		P_{OVER2}	0			dBm	3

Notes:

1. Refer to Tab. 1.
2. With both internal CDRs ON.
3. Measured with worst ER=8.2dB; $2^{31} - 1$ PRBS.
4. Bit rates below 9.83Gb/s are supported with the internal CDRs in bypass mode. Please see Sec. X for additional details.
5. 800ps/nm max chromatic dispersion tolerance over 40km of G.652 single mode fiber
6. Measured with worst ER=8.2dB; $2^7 - 1$ PRBS.

V. General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Data Rate	BR	1.2288		11.3176	Gb/sec	1
Max. Supported Link Length	L_{MAX1}			40	km	2

Notes:

1. Tested with a $2^{31} - 1$ PRBS pattern at the BER defined in Table IV.
2. Over G.652 single mode fiber.

Timing Parameters

Parameter	Symbol	Min	Max	Units	Ref.
Time to initialize cooled module	$t_{start_up_cooled}$		10	s	

VII. Environmental Specifications

Finisar FTLX3671DTCxx's operating case temperature range:

Environmental Specifications	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	-40		85	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

The FTLF8538P5BCz transceivers are RoHS compliant. Copies of certificates are available from II-VI Incorporated upon request.

FTLF8538P5BCz transceiver modules are Class 1 laser eye safety compliant per IEC 60825-1.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

VIII. Digital Diagnostic Functions

Finisar FTLX3671MTCxx SFP+ transceivers support the 2-wire serial communication protocol as defined in the SFP MSA¹. It is very closely related to the memory map defined in the GBIC standard, with the same electrical specifications.

The standard SFP serial ID provides access to identification information that describes the transceiver's capabilities, standard interfaces, manufacturer, and other information.

Additionally, Finisar SFP+ transceivers provide an enhanced digital diagnostic monitoring interface, which allows real-time access to device operating parameters such as transceiver temperature, laser bias current, transmitted optical power, received optical power and transceiver supply voltage. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The SFP MSA defines a 256-byte memory map that is accessible over a 2-wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is identical to, and is thus fully backward compatible with both the GBIC Specification and the SFP Multi Source Agreement. The complete interface is described in Finisar Application Note AN-2030: "Digital Diagnostics Monitoring Interface for SFP Optical Transceivers"⁷.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through a 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL, Mod Def 1) is generated by the host. The positive edge clocks data into the SFP transceiver into those segments of the E²PROM that are not write-protected. The negative edge clocks data from the SFP transceiver. The serial data signal (SDA, Mod Def 2) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially.

For more information, please see the SFP MSA documentation⁶ and Finisar Application Note AN-2030.

Please note that evaluation board FDB-1027 is available with Finisar ModDEMO software that allows simple to use communication over the 2-wire serial interface.

IX. Digital Diagnostic Specifications

FTLX3671MTCxx transceivers can be used in host systems that require either internally or externally calibrated digital diagnostics.

Parameter	Symbol	Units	Min	Max	Accuracy	Ref.
Transceiver temperature	ΔD_{DDTemp}	°C	-40	+85	±5°C	1
Transceiver supply voltage	$\Delta D_{DDVoltage}$	V	2.8	4.0	±3%	
Transmitter bias current	ΔD_{DDBias}	mA	0	127	±10%	2
Transmitter output power	$\Delta D_{DDTx-Power}$	dBm	-2	+3	±2dB	
Receiver average optical input power	$\Delta D_{DDRx-Power}$	dBm	-18	+1	±2dB	

Notes:

1. Internally measured

2. The accuracy of the Tx bias current is 10% of the actual current from the laser driver to the laser

X. Internal CDRs (retimers) Locking Modes

The FTLX3671MTCxx is equipped with internal receiver and the transmitter retimers. The host can set the either retimer to lock between 9.835 and 11.31 Gb/s, or in by-pass mode, via the rate select pins or the soft bits (logic OR). The different locking modes are shown in the following logic table:

R/S 0	R/S 1	CDR's Locking Mode
Logic OR of: pin 7 & bit 110.3	Logic OR of: pin 9 & bit 118.3	
Low or 0	Low or 0	Tx & Rx CDR's in bypass mode
Low or 0	High or 1	Tx CDR is in bypass mode. Rx CDR locks at 10G (9.83-11.3Gb/s)
High or 1	Low or 0	Tx & Rx CDR's in bypass mode
High or 1	High or 1	Both CDR's lock at 10G (9.83-11.3Gb/s) The bits 110.3 and 118.3 are set to 1 by default at power-up

The RS0 and RS1 pins are internally pulled-down to ground as per [1]. The soft bits 110.3 and 118.3 are both set to "1" at the transceiver power-up, to select the 10G locking mode by default. The host can change this configuration via the 2-wire communication as described in the SFP MSA [1]. Alternative configurations can be factory set upon request. Please refer to Finisar for additional details.

X. SFF-8431 Power-up Sequence

The typical power consumption of the FTLX3671MTCxx exceeds the limit of 1.5W specified for the Power Level II transceivers [1], for which a power-up sequence is recommended. However, the FTLX3671MTCxx is factory set to power-up directly to its operating conditions in Power Level Mode II. Upon request, it can be factory set to follow the power-up sequence specified for transceivers exceeding 1W, as per [1]. In power level

I, the FTLX3671MTCxx does not carry traffic, but the 2-wire serial communication is active.

Please refer to [1,3] and Finisar Application Note AN-2124 for additional details.

X. Mechanical Specifications

Finisar FTLX3671MTCxx SFP+ transceivers are compatible with the SFF-8432 specification for improved pluggable form factor, and shown here for reference purposes only. Bail color is red.

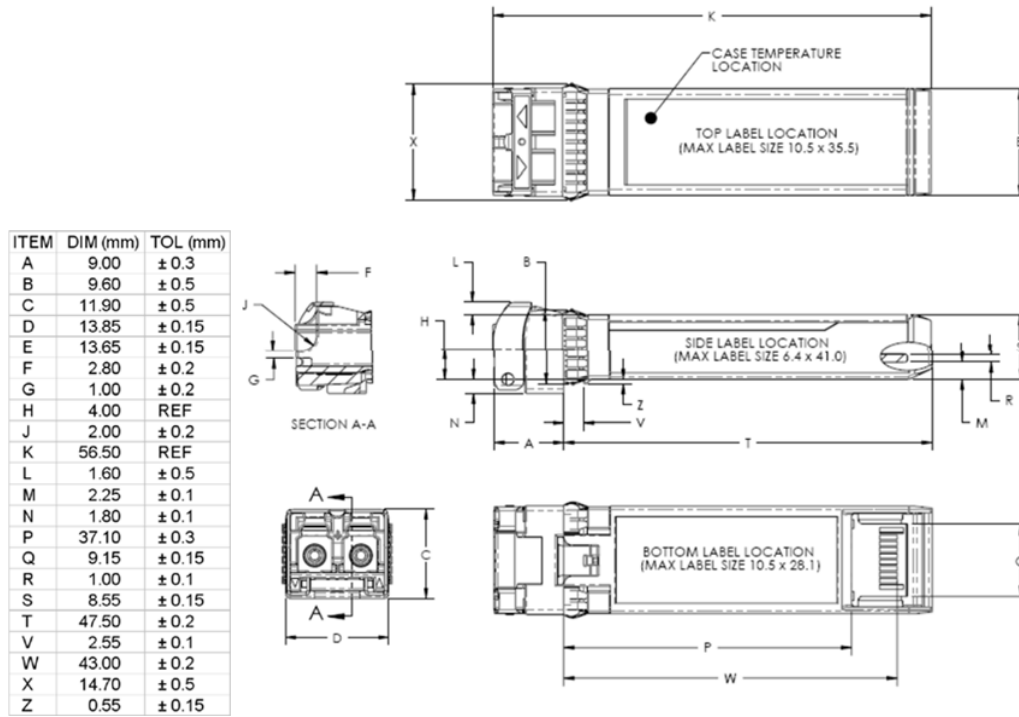


Figure 2. Mechanical Dimensions

Note: the option of the label on the top side of the transceiver is not recommended.

XIII. Host Board SFP+ Connector Recommendations

- △ Datum and Basic Dimension Established by Customer
- △ Rads and Vias are Chassis Ground, 11 Places
- △ Through Holes are Unplated

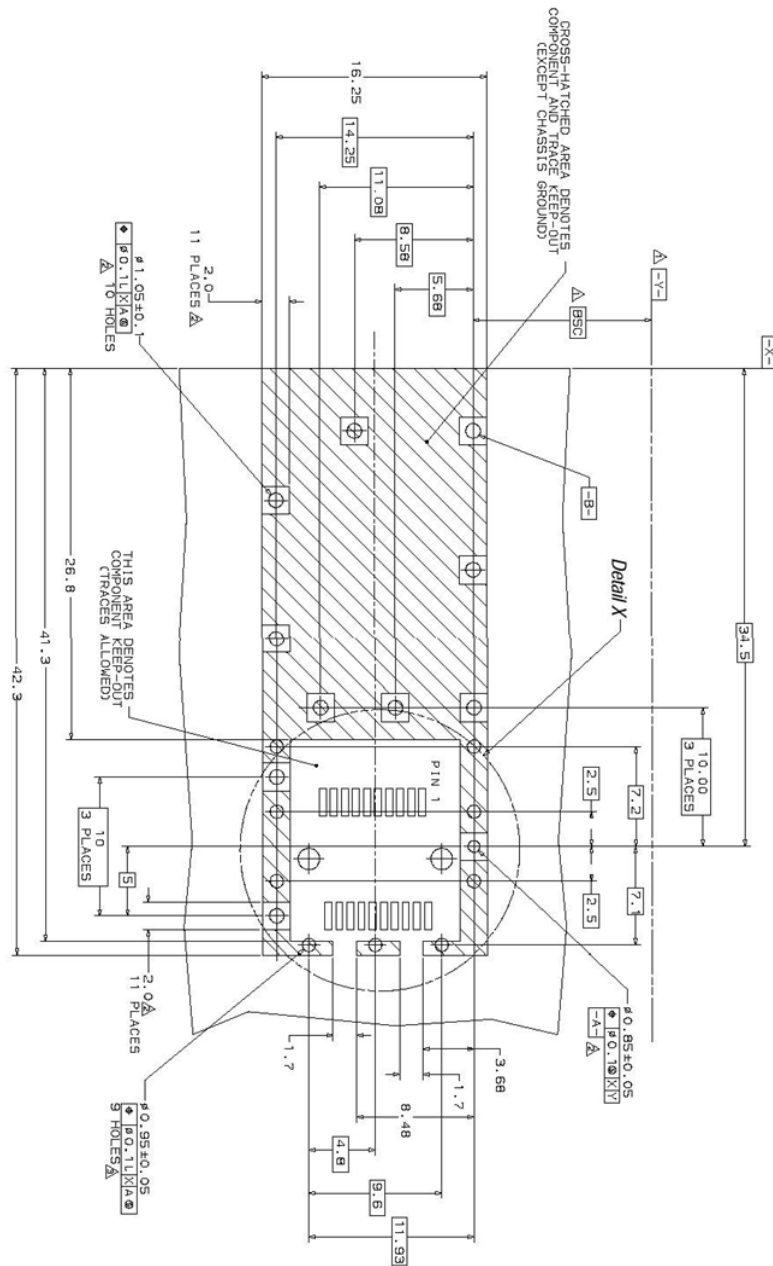
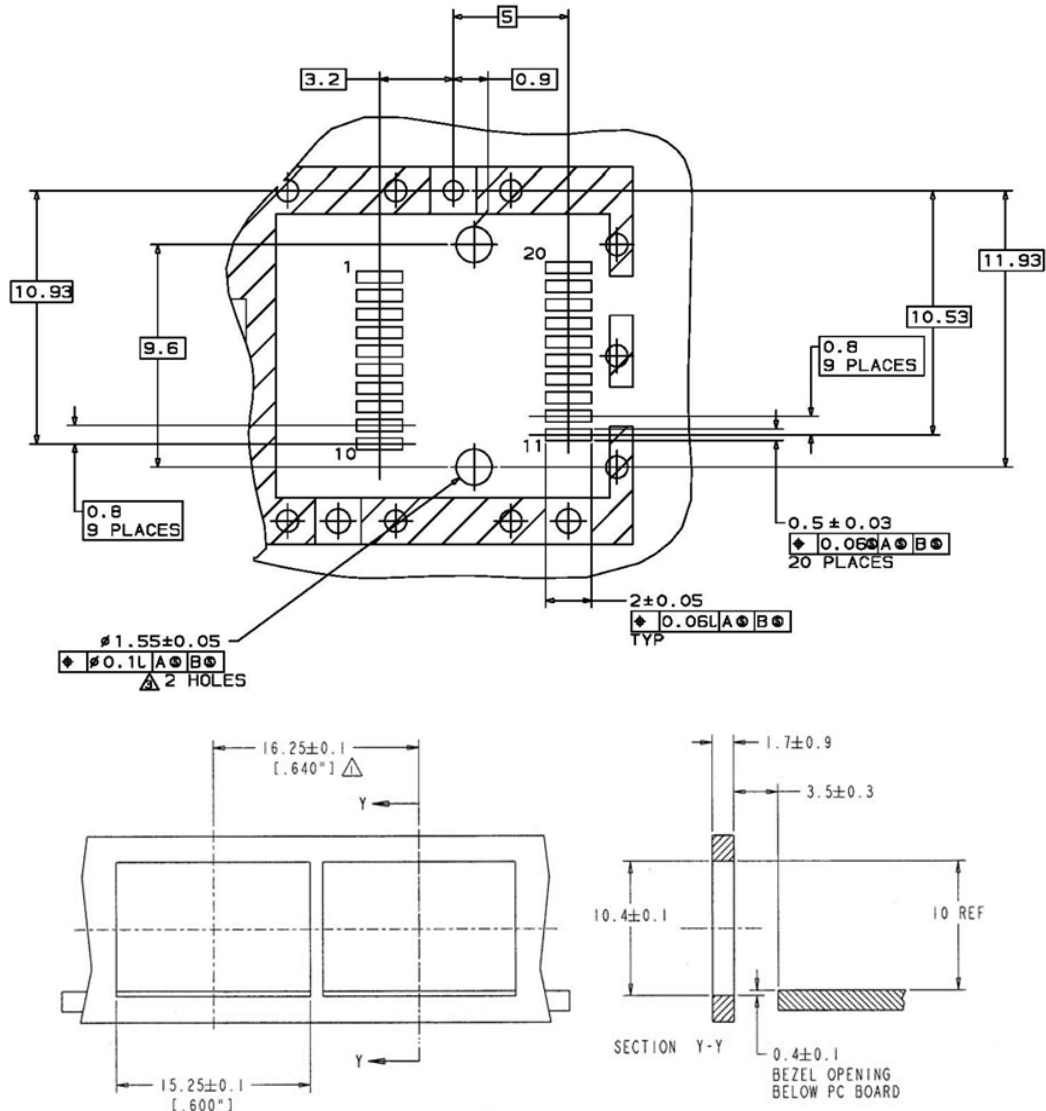


Figure 3. PCB Layout and Bezel Recommendations, as per [9]



NOTES:

△ MINIMUM PITCH ILLUSTRATED, ENGLISH DIMENSIONS ARE FOR REFERENCE ONLY

2. NOT RECOMMENDED FOR PCI EXPANSION CARD APPLICATIONS

Figure 4.

XIII. Host-Module Interface Diagram

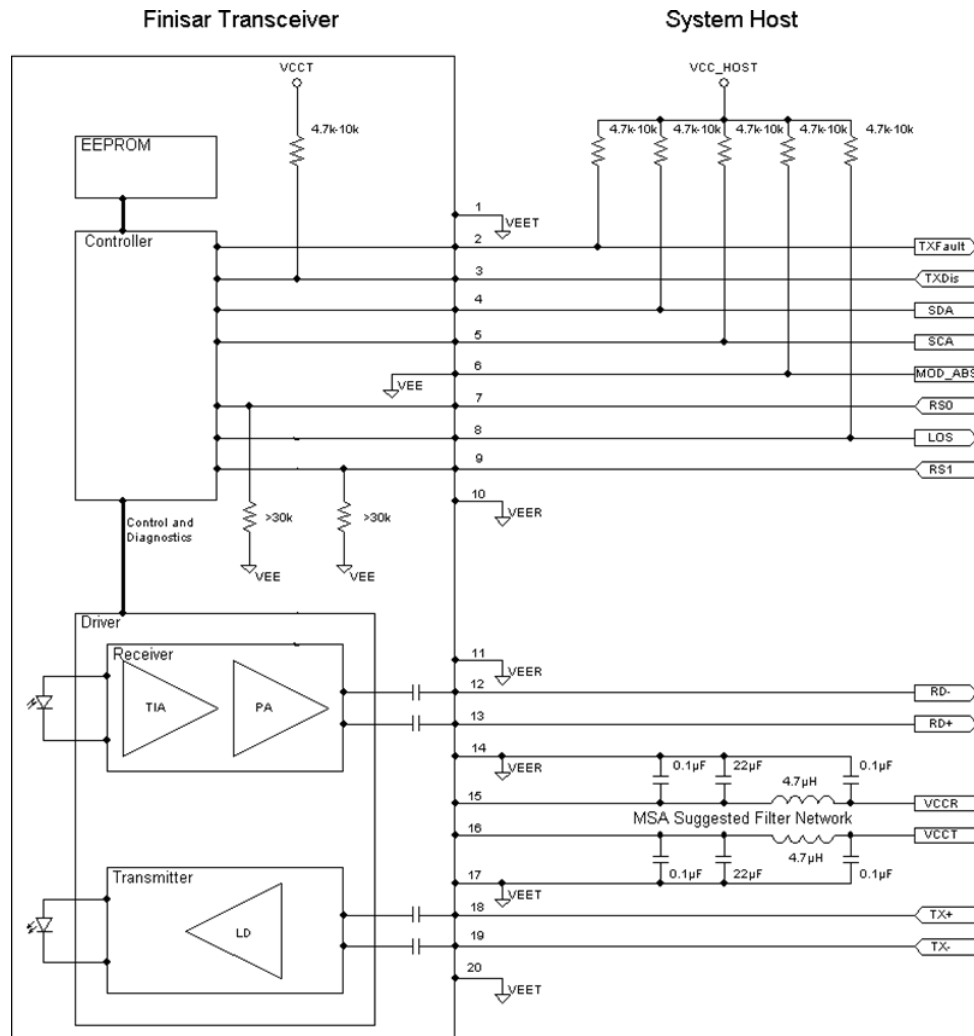


Figure 5

XIV. References

1. "Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module 'SFP+ '", SFF Document Number SFF-8431, Revision 4.1.
2. "Improved Pluggable Form factor", SFF Document Number SFF-8432, Revision 4.2, April 18, 2007.
3. "Digital Diagnostics Monitoring Interface for Optical Transceivers". SFF Document Number SFF-8472, Revision 12.2, November 21, 2014.
4. Directive 2011/65/EU of the European Parliament and of the Council "on the restriction of the use of certain hazardous substances in electrical and electronic equipment". Certain products may use one or more exemption as allowed by the directive.
5. "Application Note AN-2038: Finisar Implementation of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.
6. Small Form-factor Pluggable (SFP) Transceiver Multi-Source Agreement (MSA)
7. "Application Note AN-2030: Digital Diagnostic Monitoring Interface for SFP Optical Transceivers"
8. "Application Note AN-2076: SFP+ Level II Power Up Sequence", Rev B
9. "Application Note AN-2124: Addendum to AN-2030 with changes from SFF-8472 revision 12.2"