Product Specification

400G-FR4 OSFP
Finisar Transceiver

FTCD4315E1PCL

PRODUCT FEATURES

- Hot-pluggable OSFP form factor
- Supports 425Gb/s aggregate bit rate
- Power dissipation <12W
- RoHS-6 compliant
- Case temperature range of 0°C to +70°C (C-temp)
- Single 3.3V power supply
- Aligned with IEEE P802.3cu
- 4x100Gb/s PAM4 serial lanes
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- LC duplex receptacle
- I2C management interface

APPLICATIONS

- 400G FR4 applications with FEC

FTCD4315E1PCL 400G FR4 OSFP transceiver modules are designed for use in 400 Gigabit Ethernet links on up to 2km of single mode fiber. They are compliant with the OSFP[1] MSA, IEEE P802.3cu[4] and portions of P802.3bs[5]. Digital diagnostic functions are available via the I2C interface, as specified by the OSFP MSA. The transceiver is RoHS-6 compliant per Directive 2011/65/EU[2] and Finisar Application Note AN-2038[3].

PRODUCT SELECTION

FTCD4315E1PCL

E:	Ethernet protocol
P:	Pull-tab type release
C:	Commercial temperature range
L:	LC duplex receptacle

I.   Pin Descriptions

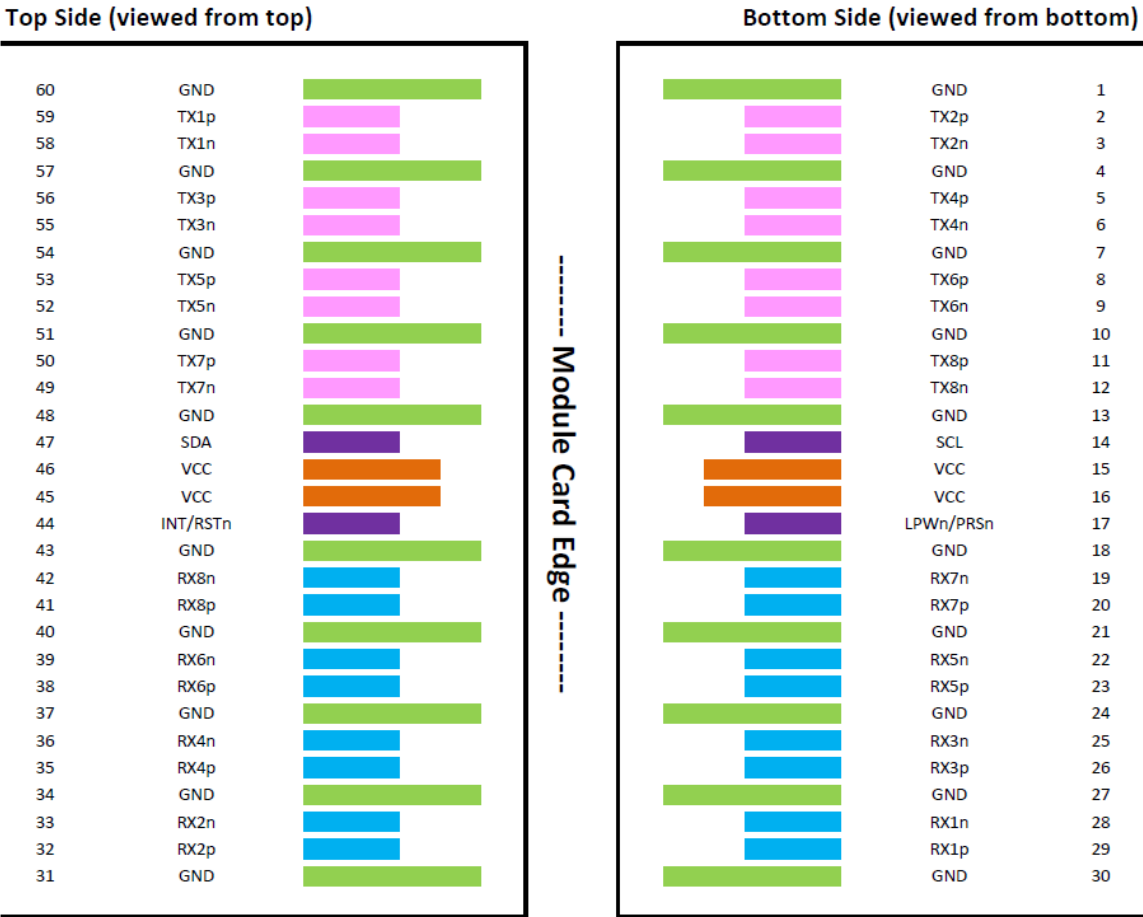The electrical pinout of the OSFP module is shown in Figure 1 below

Top Side (viewed from top)

Pin	Signal
60	GND
59	TX1p
58	TX1n
57	GND
56	TX3p
55	TX3n
54	GND
53	TX5p
52	TX5n
51	GND
50	TX7p
49	TX7n
48	GND
47	SDA
46	VCC
45	VCC
44	INT/RSTn
43	GND
42	RX8n
41	RX8p
40	GND
39	RX6n
38	RX6p
37	GND
36	RX4n
35	RX4p
34	GND
33	RX2n
32	RX2p
31	GND

------- Module Card Edge -------

Bottom Side (viewed from bottom)

Signal	Pin
GND	1
TX2p	2
TX2n	3
GND	4
TX4p	5
TX4n	6
GND	7
TX6p	8
TX6n	9
GND	10
TX8p	11
TX8n	12
GND	13
SCL	14
VCC	15
VCC	16
LPWn/PRSn	17
GND	18
RX7n	19
RX7p	20
GND	21
RX5n	22
RX5p	23
GND	24
RX3n	25
RX3p	26
GND	27
RX1n	28
RX1p	29
GND	30

Figure 1 – OSFP compliant connector (per OSFP MSA)

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

II.　　General Product Characteristics

Parameter	Value	Unit	Notes
Module Form Factor	OSFP		
Maximum Aggregate Data Rate	425	Gb/s	
Protocols Supported	400G Ethernet		
Maximum Power Consumption per End	12	Watts	1
Management Interface	Serial, I2C-based, 1 MHz maximum frequency		

Data Rate Specifications	Symbol	Min	Typ	Max	Units	Notes
Bit Error Ratio	BER			2.4E-4		2
Maximum Supported Distances						
Fiber Type						
SMF per G.652	Lmax1	0.002		2	km	

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. As defined by IEEE P802.3cu.

III.   Absolute Maximum Ratings

Module performance is not guaranteed beyond the operating range (see Section VII).
Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	-0.3		4.0	V	
Storage Temperature	T_S	-40		+85	°C	
Case Operating Temperature	T_{OP}	0		+70	°C	C-temp
Relative Humidity	RH	15		85	%	1
Receiver Damage Threshold, per Lane	P_{Rdmg}	4.5			dBm	

Notes:
1. Non-condensing.

IV.   Electrical Characteristics (EOL, T_{OP} = 0 to +70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			3.828	A	
Module total power	P			12	W	1
Transmitter						
Signaling rate per lane			26.5625± 100 ppm.		Gbd	
Differential data input voltage per lane	Vin,pp,diff	900			mV	2
Differential input return loss		Per equation (83E–5) IEEE802.3bm			dB	
Differential to common mode input return loss		Per equation (83E–6) IEEE802.3bm			dB	
Differential termination mismatch				10	%	
Module stress input test		Per 120E.3.4.1 IEEE802.3bs				3
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	4
Receiver						
Signaling rate per lane			26.5625± 100 ppm.		Gbd	
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	dB	
Differential output return loss		Per equation 83E-2 IEEE802.3bm				
Common to differential mode conversion return loss		Per equation 83E-3 IEEE802.3bm				
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage (min)		-350		2850	mV	4

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
3. Meets specified BER
4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

V.   Optical Characteristics (EOL, T_{OP} = 0 to +70 °C, V_{CC} = 3.135 to 3.465 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Signaling rate (each lane (range)		53.125 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelength (range)		1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Side-mode suppression ratio (SMSR)		30			dB	
Total average launch power				10.4	dBm	
Average launch power, each lane				4.4	dBm	
Average launch power, each lane		-3.2			dBm	1
Difference in launch power between any two lanes (OMAouter) max				3.9	dB	
Outer Optical Modulation Amplitude (OMAouter), each lane min for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.4 dB		-0.2 -1.6 + TDECQ		3.7	dBm dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane				3.4	dB	
TDECQ – TECQ				2.5	dB	
Average launch power of OFF transmitter, each lane				-16	dBm	
Extinction ratio		3.5			dB	
Transmitter transition time				17	pS	
Transmitter over/under-shoot				22	%	
Transmitter power excursion				1.8	dBm	
$RIN_{17.1}OMA$				-136	dB/Hz	
Optical return loss tolerance				17.1	dB	
Transmitter reflectance				-26	dB	2

Notes:
1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Transmitter reflectance is defined looking into the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver						
Signaling rate (each lane (range)			53.125 ± 100 ppm		GBd	
Modulation format			PAM4			
Lane wavelength (range)		1264.5 1284.5 1304.5 1324.5	1271 1291 1311 1331	1277.5 1297.5 1317.5 1337.5	nm	
Damage threshold, each lane			5.4		dBm	1
Average receive power, each lane				4.4	dBm	
Average receive power, each lane		-7.2			dBm	2
Receive power (OMAouter), each lane				3.7	dBm	
Difference in receive power between any two lanes (OMAouter)				4.1	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMA$_{outer}$), each lane (max) for SECQ < 1.4 dB for 1.4 dB ≤ SECQ ≤ 3.4 dB				-4.6 -6 + SECQ	dBm dBm	
Receiver sensitivity (OMAouter), each lane				-2.6		3
Conditions of stressed receiver sensitivity test:[4]						
Stressed eye closure for PAM4 (SECQ), lane under test			3.4		dB	4
OMAouter of each aggressor lane			1.5		dBm	

Notes:
1. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
3. Measured with conformance test signal at TP3 (see 151.8.13) for the BER specified in 151.1.1.
4. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

VI.   Memory Map and Control Registers

Per CMIS4.0. See Finisar Application Note AN-21xx (TBD)..

VII.   Environmental Specifications

Finisar FTCD4315E1PCL FR4 OSFP transceivers have a max. operating case temperature range of 0°C to +70°C.

| Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T$_{op}$	0		+70	°C	C-temp
Storage Temperature	T$_{sto}$	-40		+85	°C	

VIII.   Regulatory Compliance

Finisar FTCD4315E1PCL FR4 OSFP transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040.10 and Laser Notice 56
Laser Eye Safety	UL/CSA/TÜV	IEC/EN 60825-1:2014 IEC/EN 60825-2: 2004+A1+A2
Electrical Safety	UL/CSA/TÜV	IEC/UL/CSA/EN 62368-1:2014

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

IX.   Mechanical Specifications

Finisar FTCD4315E1PCL FR4 OSFP transceivers are compatible with the OSFP Specification for pluggable form factor modules.
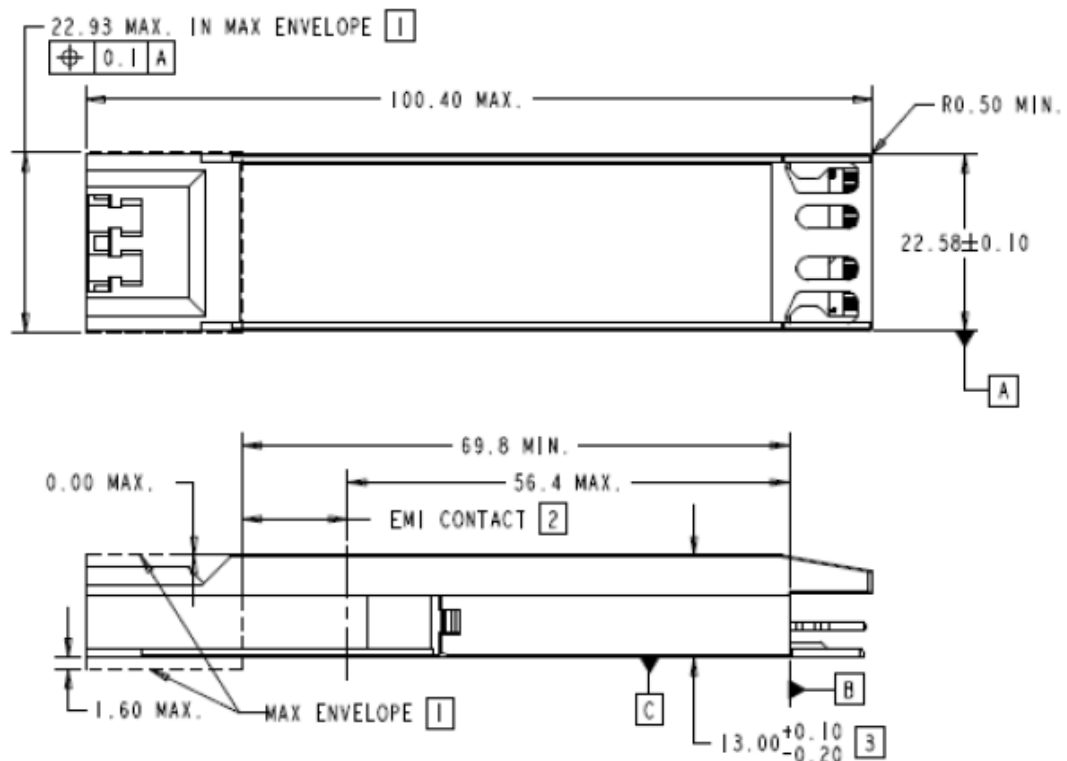
NOTES:

[1] FRONT OF THE MODULE, PULL TAB AND OTHER COMPONENTS CAN EXTEND 1.60 mm MAX FROM THE BOTTOM AND 0.00 mm FROM THE TOP WITH UP TO 22.93MM WIDTH IN THE MAX ENVELOPE SHOWN.

[2] INDICATED SURFACES (ALL 4 SIDES) TO BE CONDUCTIVE FOR CONNECTION TO CHASSIS GROUND.

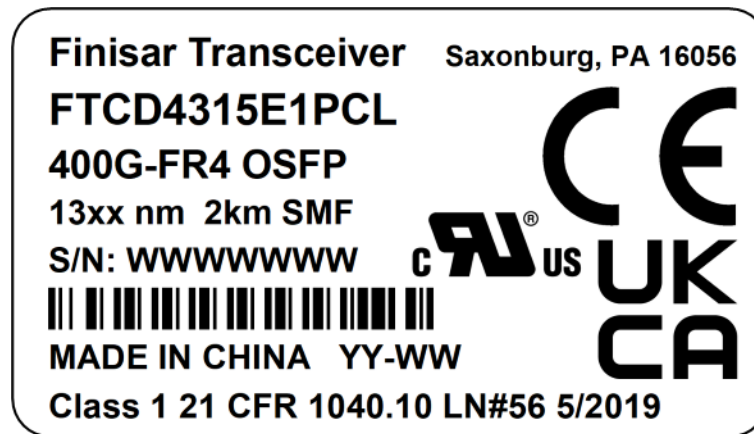[3] APPLIES FROM THE TOP OF THE MODULE TO THE BOTTOM OF THE MODULE, INSIDE THE CAGE.

Figure 2. FTCD4315E1PCL Mechanical Dimensions.

Figure 3. Product Label (Not to Scale)
"Made in Malaysia" version also available under PN "FTCD4315E1PCL-1Y"

X.   References

1. OSFP Specification for OSFP Octal small form factor pluggable module

2. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment" as well as Commission Delegated Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU. Certain products may use one or more exemptions as allowed by the Directive.

3. Application Note AN-2038: "II-VI Implementation of RoHS Compliant Transceivers".

4. IEEE P802.3cu 400GBASE-FR4.

5. IEEE P802.3bs, 400GAUI-8 Interface.

XI.   For More Information

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