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Application Note AN-2152

100G QSFP28 LR4 EEPROM Application Note Rev D

Introduction

The purpose of this application note is to document the EEPROM contents of Finisar's 100 Gigabit Ethernet QSFP28 LR4 modules. This application note applies to 100GE (4X25G) QSFP28 LR4 Finisar part number FTLC115yRDxL and to 100G (4X25G Ethernet) - 112G (4X28G OTN) multirate QSFP28 SR4 Finisar part number FTLC115ySDxL (where y is "1" or "4" and x is "N" or "P")

All registers are supported per SFF-8636 REV 2.7 Common Management Interface, which are applicable for a SM (separable module) and per SFF-8024 REV 3.9 Specification for SFF Committee Cross Reference to Industry Products. The EEPROM Mapping below is meant to be an inclusive listing of what is supported by the transceiver.

Applicable Documents, Standards and MSA's

a. SFF-8636, QSFP28 100G Common Management Interface Rev 2.7, January 26th 2016.
b. SFF-8679, QSFP 4x Base Electrical Specification Rev 1.7, August 12, 2014
c. SFF-8024, SFF Committee Cross Reference, Rev 3.9, March 14th 2016
d. IEEE802.3bm D3p3

How to use this Application Note

Please refer to the SFF-8636 and SFF-8024 documents for information on the available EEPROM memory content, then compare with what is listed below. Register content specific to FTLC115ySDxL will be marked in parentheses ( ).
The addresses which are not implemented are highlighted in yellow. These are optional per the MSA, thus not required to be implemented.

Content

The following are the EEPROM maps of the QSFP+ transceiver:
Legend:

No highlight = implemented.

Yellow highlight = Optional / not implemented

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ADDRESS A0H LOWER PAGE 00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
0	0		RO	Identifier	QSFP28 (SFF-8636)	11
1	1		RO	Revision Compliance	SFF-8636 Rev 2.5	7
2	2	7 ~ 3	RO	RESERVED		
		2		Flat_mem: Upper memory flat or paged. Flat memory: 0= paging, 1= Page 00h only		
		1		IntL: Digital state of the IntL Interrupt output pin (if pin supported)		
		0		Data_Not_Ready		
3	3	7	RO	L-TX4 LOS. Latched TX LOS indicator, channel 4		
		6		L-TX3 LOS. Latched TX LOS indicator, channel 3		
		5		L-TX2 LOS. Latched TX LOS indicator, channel 2		
		4		L-TX1 LOS. Latched TX LOS indicator, channel 1		
		3		L-RX4 LOS. Latched TX LOS indicator, channel 4		
		2		L-RX3 LOS. Latched TX LOS indicator, channel 3		
		1		L-RX2 LOS. Latched TX LOS indicator, channel 2		
		0		L-RX1 LOS. Latched TX LOS indicator, channel 1		
4	4	7	RO	Latched TX, Adaptive EQ fault indicator, channel 4 (if supported)		
		6		Latched TX, Adaptive EQ fault indicator, channel 3 (if supported)		
		5		Latched TX, Adaptive EQ fault indicator, channel 2 (if supported)		
		4		Latched TX, Adaptive EQ fault indicator, channel 1 (if supported)		
		3		Latched TX Transmitter/Laser fault indicator, channel 4		
		2		Latched TX Transmitter/Laser fault indicator, channel 3		
		1		Latched TX Transmitter/Laser fault indicator, channel 2		
		0		Latched TX Transmitter/Laser fault indicator, channel 1		
5	5	7	RO	Latched TX CDR LOL indicator, ch 4		
		6		Latched TX CDR LOL indicator, ch 3		
		5		Latched TX CDR LOL indicator, ch 2		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		4		Latched TX CDR LOL indicator, ch 1		
		3		Latched RX CDR LOL indicator, ch 4		
		2		Latched RX CDR LOL indicator, ch 3		
		1		Latched RX CDR LOL indicator, ch 2		
		0		Latched RX CDR LOL indicator, ch 1		
6	6	7	RO	Latched high temperature alarm		
		6		Latched low temperature alarm		
		5		Latched high temperature warning		
		4		Latched low temperature warning		
		3 ~ 1		Reserved		
		0		Initialization complete flag: This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at byte 6, bit 0 is implemented independent of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module.		
7	7	7	RO	Latched high supply voltage alarm		
		6		Latched low supply voltage alarm		
		5		Latched high supply voltage warning		
		4		Latched low supply voltage warning		
		3 ~ 0		Reserved		
8	8			Vendor Specific		
9	9	7	RO	Latched high RX power alarm, channel 1		
		6		Latched low RX power alarm, channel 1		
		5		Latched high RX power warning, channel 1		
		4		Latched low RX power warning, channel 1		
		3		Latched high RX power alarm, channel 2		
		2		Latched low RX power alarm, channel 2		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		1		Latched high RX power warning, channel 2		
		0		Latched low RX power warning, channel 2		
10	0A	7	RO	Latched high RX power alarm, channel 3		
		6		Latched low RX power alarm, channel 3		
		5		Latched high RX power warning, channel 3		
		4		Latched low RX power warning, channel 3		
		3		Latched high RX power alarm, channel 4		
		2		Latched low RX power alarm, channel 4		
		1		Latched high RX power warning, channel 4		
		0		Latched low RX power warning, channel 4		
11	0B	7	RO	Latched high TX bias alarm, channel 1		
		6		Latched low TX bias alarm, channel 1		
		5		Latched high TX bias warning, channel 1		
		4		Latched low TX bias warning, channel 1		
		3		Latched high TX bias alarm, channel 2		
		2		Latched low TX bias alarm, channel 2		
		1		Latched High TX bias warning, channel 2		
		0		Latched low TX bias warning, channel 2		
12	0C	7	RO	Latched high TX bias alarm, channel 3		
		6		Latched low TX bias alarm, channel 3		
		5		Latched high TX bias warning, channel 3		
		4		Latched low TX bias warning, channel 3		
		3		Latched high TX bias alarm, channel 4		
		2		Latched low TX bias alarm, Channel 4		
		1		Latched high TX bias warning, channel 4		
		0		Latched low TX bias warning, channel 4		
13	0D	7	RO	Latched high TX Power alarm, channel 1		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		6		Latched low TX Power alarm, channel 1		
		5		Latched high TX Power warning, channel 1		
		4		Latched low TX Power warning, channel 1		
		3		Latched high TX Power alarm, channel 2		
		2		Latched low TX Power alarm, channel 2		
		1		Latched High TX Power warning, channel 2		
		0		Latched low TX Power warning, channel 2		
14	0E	7	RO	Latched high TX Power alarm, channel 3		
		6		Latched low TX Power alarm, channel 3		
		5		Latched high TX Power warning, channel 3		
		4		Latched low TX Power warning, channel 3		
		3		Latched high TX Power alarm, channel 4		
		2		Latched low TX Power alarm, Channel 4		
		1		Latched high TX Power warning, channel 4		
		0		Latched low TX Power warning, channel 4		
15	0F		RO	Reserved		
16	10		RO	Reserved		
17	11		RO	Reserved		
18	12		RO	Reserved		
19	13		RO	Vendor Specific		
20	14		RO	Vendor Specific		
21	15		RO	Vendor Specific		
22	16		RO	Internally measured temperature (MSB)		
23	17		RO	Internally measured temperature (LSB)		
24	18		RO	Reserved		
25	19		RO	Reserved		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
26	1A		RO	Internally measured supply voltage (MSB)		
27	1B		RO	Internally measured supply voltage (LSB)		
28	1C		RO	Reserved		
29	1D		RO	Reserved		
30	1E		RO	Vendor Specific		
31	1F		RO	Vendor Specific		
32	20		RO	Vendor Specific		
33	21		RO	Vendor Specific		
34	22		RO	Internally measured RX input power, channel 1 (MSB)		
35	23		RO	Internally measured RX input power, channel 1 (LSB)		
36	24		RO	Internally measured RX input power, channel 2 (MSB)		
37	25		RO	Internally measured RX input power, channel 2 (LSB)		
38	26		RO	Internally measured Rx input power, channel 3 (MSB)		
39	27		RO	Internally measured Rx input power, channel 3 (LSB)		
40	28		RO	Internally measured Rx input power, channel 4 (MSB)		
41	29		RO	Internally measured Rx input power, channel 4 (LSB)		
42	2A		RO	Internally measured TX bias, channel 1 (MSB)		
43	2B		RO	Internally measured TX bias, channel 1 (LSB)		
44	2C		RO	Internally measured TX bias, channel 2 (MSB)		
45	2D		RO	Internally measured TX bias, channel 2 (LSB)		
46	2E		RO	Internally measured TX bias, channel 3 (MSB)		
47	2F		RO	Internally measured TX bias, channel 3 (LSB)		
48	30		RO	Internally measured TX bias, channel 4 (MSB)		
49	31		RO	Internally measured TX bias, channel 4 (LSB)		
50	32		RO	Internally measured TX Power, channel 1 (MSB)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
51	33		RO	Internally measured TX Power, channel 1 (LSB)		
52	34		RO	Internally measured TX Power, channel 2 (MSB)		
53	35		RO	Internally measured TX Power, channel 2 (LSB)		
54	36		RO	Internally measured TX Power, channel 3 (MSB)		
55	37		RO	Internally measured TX Power, channel 3 (LSB)		
56	38		RO	Internally measured TX Power, channel 4 (MSB)		
57	39		RO	Internally measured TX Power, channel 4 (LSB)		
58	3A		RO	Reserved Channel Monitor set		
59	3B		RO	Reserved Channel Monitor set		
60	3C		RO	Reserved Channel Monitor set		
61	3D		RO	Reserved Channel Monitor set		
62	3E		RO	Reserved Channel Monitor set		
63	3F		RO	Reserved Channel Monitor set		
64	40		RO	Reserved Channel Monitor set		
65	41		RO	Reserved Channel Monitor set		
66	42		RO	Reserved Channel Monitor set		
67	43		RO	Reserved Channel Monitor set		
68	44		RO	Reserved Channel Monitor set		
69	45		RO	Reserved Channel Monitor set		
70	46		RO	Reserved Channel Monitor set		
71	47		RO	Reserved Channel Monitor set		
72	48		RO	Reserved Channel Monitor set		
73	49		RO	Reserved Channel Monitor set		
74	4A			Vendor Specific		
75	4B			Vendor Specific		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
76	4C			Vendor Specific		
77	4D			Vendor Specific		
78	4E			Vendor Specific		
79	4F			Vendor Specific		
80	50			Vendor Specific		
81	51			Vendor Specific		
82	52			Reserved		
83	53			Reserved		
84	54			Reserved		
85	55			Reserved		
86	56	7 ~ 4		Reserved		
		3	RW	Tx4 Disable		
		2	RW	Tx3 Disable		
		1	RW	Tx2 Disable		
		0	RW	Tx1 Disable		
87	57	7	RW	Rx4_Rate_select MSB		AA
		6	RW	Rx4_Rate_select LSB		
		5	RW	Rx3_Rate_select MSB		
		4	RW	Rx3_Rate_select LSB		
		3	RW	Rx2_Rate_select MSB		
		2	RW	Rx2_Rate_select LSB		
		1	RW	Rx1_Rate_select MSB		
		0	RW	Rx1_Rate_select LSB		
88	58	7	RW	Tx4_Rate_select MSB		AA
		6	RW	Tx4_Rate_select LSB		
		5	RW	Tx3_Rate_select MSB		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		4	RW	Tx3_Rate_select LSB		
		3	RW	Tx2_Rate_select MSB		
		2	RW	Tx2_Rate_select LSB		
		1	RW	Tx1_Rate_select MSB		
		0	RW	Tx1_Rate_select LSB		
89	59		RW	Software Application Select per SFF-8079, Rx Channel 4		
90	5A		RW	Software Application Select per SFF-8079, Rx Channel 3		
91	5B		RW	Software Application Select per SFF-8079, Rx Channel 2		
92	5C		RW	Software Application Select per SFF-8079, Rx Channel 1		
93	5D	7 ~ 3		Reserved		
		2	RW	High Power Class Enable (Classes 5 - 7). When set (= 1b) enables Power Classes 5 to 7 in Byte 129 to exceed 3.5W. When cleared (= 0b), modules with Power classes 5 to 7 must dissipate less than 3.5W (but are not required to be fully functional). Default 0.		
		1	RW	Power set to Low Power Mode Default 0		
		0	RW	Override of LP mode signal setting the power mode with software		
94	5E		RW	Tx4_Application_Select		
95	5F		RW	Tx3_Application_Select		
96	60		RW	Tx2_Application_Select		
97	61		RW	Tx1_Application_Select		
98	62	7	RW	Tx4_CDR_control (1b = CDR on, 0b = CDR off)		Default FF
		6	RW	Tx3_CDR_control (1b = CDR on, 0b = CDR off)		
		5	RW	Tx2_CDR_control (1b = CDR on, 0b = CDR off)		
		4	RW	Tx1_CDR_control (1b = CDR on, 0b = CDR off)		
		3	RW	Rx4_CDR_control (1b = CDR on, 0b = CDR off)		
		2	RW	Rx3_CDR_control (1b = CDR on, 0b = CDR off)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		1	RW	Rx2_CDR_control (1b = CDR on, 0b = CDR off)		
		0	RW	Rx1_CDR_control (1b = CDR on, 0b = CDR off)		
99	63			Reserved		
100	64	7	RW	Masking bit Tx4 LOS		
		6	RW	Masking bit-Tx3 LOS		
		5	RW	Masking bit-Tx2 LOS		
		4	RW	Masking bit-Tx1 LOS		
		3	RW	Masking bit-Rx4 LOS		
		2	RW	Masking bit-Rx3 LOS		
		1	RW	Masking bit-Rx2 LOS		
		0	RW	Masking bit-Rx1 LOS		
101	65	7	RW	Masking bit Tx4 Adapt EQ Fault		
		6	RW	Masking bit Tx3 Adapt EQ Fault		
		5	RW	Masking bit Tx2 Adapt EQ Fault		
		4	RW	Masking bit Tx1 Adapt EQ Fault		
		3	RW	Masking bit Tx4 Transmitter Fault		
		2	RW	Masking bit Tx3 Transmitter Fault		
		1	RW	Masking bit Tx2 Transmitter Fault		
		0	RW	Masking bit Tx1 Transmitter Fault		
102	66	7	RW	Masking bit -Tx4 CDR LOL		
		6	RW	Masking bit -Tx3 CDR LOL		
		5	RW	Masking bit -Tx2 CDR LOL		
		4	RW	Masking bit -Tx1 CDR LOL		
		3	RW	Masking bit -Rx4 CDR LOL		
		2	RW	Masking bit -Rx3 CDR LOL		
		1	RW	Masking bit -Rx2 CDR LOL		
		0	RW	Masking bit -Rx1 CDR LOL		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
103	67	7	RW	Masking Bit for high Temperature alarm		
		6	RW	Masking Bit for low Temperature alarm		
		5	RW	Masking Bit for high Temperature warning		
		4	RW	Masking Bit for low Temperature warning		
		3 ~ 0	RW	Reserved		
104	68	7	RW	Masking Bit for high Vcc alarm		
		6	RW	Masking Bit for low Vcc alarm		
		5	RW	Masking Bit for high Vcc warning		
		4	RW	Masking Bit for low Vcc warning		
		3 ~ 0	RW	Reserved		
105	69			Vendor Specific		
106	6A			Vendor Specific		
107	6B		RW	Reserved		
108	6C		RO	Most significant byte of propagation delay		
109	6D		RO	Least significant byte of propagation delay		
110	6E	7 ~ 4	RO	Advanced Low Power Mode		
		3	RO	Far Side Managed: A value of 1 indicates that the far end is managed and complies with SFF-8636.		
		2 ~ 0	RO	Min Operating Voltage		
111	6F			Assigned for use by PCI Express		
112	70			Assigned for use by PCI Express		
113	71	7		Reserved		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		6 ~ 4	RO	=000 Far end is unspecified =001 Cable with single far end with 4 channels implemented, or separable module with 4-channel connector =010 Cable with single far end with 2 channels implemented, or separable module with 2-channel connector =011 Cable with single far end with 1 channel implemented, or separable module with 1-channel connector =100 4 far ends with 1 channel implemented in each (i.e. 4x1 break out) =101 2 far ends with 2 channels implemented in each (i.e. 2x2 break out) =110 2 far ends with 1 channel implemented in each (i.e. 2x1 break out)		
		3 ~ 0	RO	Near End Implementation: Bit 0 =0 Channel 1 implemented =1 Channel 1 not implemented Bit 1 =0 Channel 2 implemented =1 Channel 2 not implemented Bit 2 =0 Channel 3 implemented =1 Channel 3 not implemented Bit 3 =0 Channel 4 implemented =1 Channel 4 not implemented		
114	72		RW	Reserved		
115	73		RW	Reserved		
116	74		RW	Reserved		
117	75		RW	Password change area		
118	76		RW	Password change area		
119	77		WO	Password change area		
120	78		WO	Password change area		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
121	79		WO	Password change area		
122	7A		WO	Password change area		
123	7B		WO	Password Entry area		
124	7C		WO	Password Entry area		
125	7D		WO	Password Entry area		
126	7E		WO	Password Entry area		
127	7F		WO	Page Select Byte		

ADDRESS A0H UPPER PAGE 00

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
128	80		RO	Identifier	QSFP28 (SFF-8636)	11
129	81	7 ~ 6	RO	Extended Identifier		CC
				00: Power Class 1 (1.5 W max)	Power Class 4 (3.5 W max)	
				01: Power Class 2 (2.0 W max)		
				10: Power Class 3 (2.5 W max)		
				11: Power Class 4 (3.5 W max)		
		5		Reserved		
		4		0: No CLEI code present in Page 02h	No CLEI code present in Page 02h	
				1: CLEI code present in Page 02h		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		3		0: No CDR in TX , 1: CDR present in TX	CDR present in Tx	
		2		0: No CDR in RX , 1: CDR present in RX	CDR present in Rx	
		1 ~ 0		00: unused (legacy setting)	Unused	
				01: Power Class 5 (4.0 W max) See Byte 93 bit 2 to enable		
				10: Power Class 6 (4.5 W max) See Byte 93 bit 2 to enable		
				11: Power Class 7 (5.0 W max) See Byte 93 bit 2 to enable		
130	82		RO	Connector Type	LC	07
131	83	7	RO	The Extended Specification Compliance: Codes are maintained in the Transceiver Management section of SFF-8024	TRUE	80
		6		10GBASE-LRM		
		5		10GBASE-LR		
		4		10GBASE-SR		
		3		40GBASE-CR4		
		2		40GBASE-SR4		
		1		40GBASE-LR4		
		0		40G Active Cable (XLPPI)		
132	84	7 ~ 3		Reserved		0
		2		OC 48, long reach		
		1		OC 48, intermediate reach		
		0		OC 48 short reach		
133	85	7		Reserved SAS		0
		6		SAS 12.0 Gbps		
		5		SAS 6.0 Gbps		
		4		SAS 3.0 Gbps		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		3 ~ 0		Reserved		
134	86	7 ~ 4		Reserved		0
		3		1000BASE-T		
		2		1000BASE-CX		
		1		1000BASE-LX		
		0		1000BASE-SX		
135	87	7		Very long distance (V)		0
		6		Short distance (S)		
		5		Intermediate distance (I)		
		4		Long distance (L)		
		3		Medium (M)		
		2		Reserved		
		1		Longwave laser (LC)		
		0		Electrical inter-enclosure (EL)		
136	88	7		Electrical intra-enclosure		0
		6		Shortwave laser w/o OFC (SN)		
		5		Shortwave laser w OFC (SL)		
		4		Longwave Laser (LL)		
		3 ~0		Reserved		
137	89	7	RO	Twin Axial Pair (TW)		0
		6		Shielded Twisted Pair (TP)		
		5		Miniature Coax (MI)		
		4		Video Coax (TV)		
		3		Multi-mode 62.5 m (M6)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		2		Multi-mode 50 m (M5)		
		1		Multi-mode 50 um (OM3)		
		0		Single Mode (SM)		
138	8A	7	RO	1200 MBytes/Sec		0
		6		800 MBytes/Sec		
		5		1600 MBytes/Sec		
		4		400 MBytes/Sec		
		3		3200 MBytes/sec		
		2		200 MBytes/Sec		
		1		Extended see Byte 192		
		0		100 Mbytes/Sec		
139	8B			Encoding	64B/66B	5
140	8C			Nominal bit rate, units of 100 Mbps. For BR > 25.4G	255	FF
141	8D	7 ~ 2	RO	Reserved		0 (02)
		1		QSFP+ Rate Select Version 2	(implemented)	
		0		QSFP+ Rate Select Version 1		
142	8E		RO	Link length supported for SMF fiber in km	10 km	0A
143	8F		RO	Link length supported for EBW 50/125 um fiber (OM3), units of 2 m	0 m	0
144	90		RO	Link length supported for 50/125 um fiber (OM2), units of 1 m	0 m	0
145	91		RO	Link length supported for 62.5/125 um fiber (OM1), units of 1 m	0 m	0
146	92		RO	Length of passive or active cable assembly (units of <=1 m) or link length supported for OM4 50/125 um fiber (units of <=2 m) as indicated by byte 147.	0 m	0
147	93	7	RO	Transmitter Technology	0	44
		6			1 = 1310 nm DFB	
		5			0	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		4			0	
		3		0: No Wavelength Control ; 1: Active Wavelength Control	0	
		2		0: Uncooled transmitter device; 1: Cooled transmitter	1 = cooled transmitter	
		1		0: Pin detector; 1: APD detector	0	
		0		0: Transmitter not Tunable ; 1: Transmitter Tunable	0	
148	94		RO	Vendor Name	F	46
149	95				I	49
150	96				N	4E
151	97				I	49
152	98				S	53
153	99				A	41
154	9A				R	52
155	9B					20
156	9C				C	43
157	9D				O	4F
158	9E				R	52
159	9F				P	50
160	A0					20
161	A1					20
162	A2					20
163	A3					20
164	A4	7 ~ 5	RO	Reserved		0
		4		EDR (20.0 Gb/s)		
		3		FDR (14.0 Gb/s)		
		2		QDR (10.0 Gb/s)		
		1		DDR (5.0 Gb/s)		
		0		SDR (2.5 Gb/s)		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
165	A5		RO	Vendor OUI: IEEE Company ID		0
166	A6					90
167	A7					65
168	A8		RO	Vendor Part Number	F	46
169	A9				T	54
170	AA				L	4C
171	AB				C	43
172	AC				1	31
173	AD				1	31
174	AE				5	35
175	AF				y = (1 or4)	31 or 34
176	B0				R (S)	52 (53)
177	B1				D	44
178	B2				x = (N or P)	4E or 50
179	B3				L	4C
180	B4					20
181	B5					20
182	B6					20
183	B7					20
184	B8			Vendor Revision	A0	41
185	B9					30
186	BA			Wavelength or Copper Cable Attenuation. (Wavelength=Value/20 in nm)	1302 nm	65
187	BB					BF
188	BC			Wavelength tolerance or Copper Cable Attenuation. (Wavelength Tol.=value/200 in nm)	1 nm	00
189	BD					CE
190	BE			Maximum Case Temperature. If 70 deg C then use 0		0

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
191	BF			Check code for base ID fields (bytes 128-190)	calculated	CHK SUM
192	C0			Link Codes: Extended Specification Compliance Codes. SFF-8024	100GBASE-LR4	3
193	C1	7 ~ 4		Reserved		07 (0F)
		3		TX Input Equalization Auto Adaptive Capable, coded 1 if implemented, else 0.	FTLC1151 N/A (FTLC1154 Implemented)	
		2		TX Input Equalization Fixed Programmable Settings, coded 1 if implemented, else 0	implemented	
		1		RX Output Emphasis Fixed Programmable Settings, coded 1 if implemented, else 0.	implemented	
		0		RX Output Amplitude Fixed Programmable Settings, coded 1 if implemented, else 0.	implemented	
194	C2	7		TX CDR On/Off Control implemented, (1b if controllable, 0b if fixed).	implemented	FF
		6		RX CDR On/Off Control implemented, (1b if controllable, 0b if fixed)	implemented	
		5		Tx CDR Loss of Lock (LOL) Flag implemented, coded 1 if implemented, else 0.	implemented	
		4		Rx CDR Loss of Lock (LOL) Flag implemented, coded 1 if implemented, else 0.	implemented	
		3		Rx Squelch Disable implemented, coded 1 if implemented, else 0	implemented	
		2		Rx Output Disable capable: coded 1 if implemented, else 0.	implemented	
		1		Tx Squelch Disable implemented: coded 1 if implemented, else 0	implemented	
		0		Tx Squelch implemented: coded 1 if implemented, else 0	implemented	
195	C3	7		Memory page 02 provided: coded 1 if implemented, else 0	implemented	DE (FE)
		6		Memory Page 01h provided: coded 1 if implemented, else 0	implemented	
		5		RATE_SELECT, 1 if implemented, else 0	FTLC1151 N/A (FTLC1154 Implemented)	
		4		Tx_DISABLE is implemented and disables the serial output	implemented	
		3		Tx_FAULT signal implemented, coded 1 if implemented, else 0	implemented	
		2		Tx Squelch implemented to reduce OMA coded 0, implemented to reduce Pave coded 1.	implemented	
		1		Tx Loss of Signal implemented, coded 1 if implemented, else 0	implemented	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		0		Reserved		
196	C4			Vendor Serial Number		41
197	C5					30
198	C6					30
199	C7					30
200	C8					30
201	C9					30
202	CA					30
203	CB					20
204	CC					20
205	CD					20
206	CE					20
207	CF					20
208	D0					20
209	D1					20
210	D2					20
211	D3					20
212	D4			Date Code	ASCII code, two low order digits of year. (00=2000).	31
213	D5					35
214	D6				ASCII code, digits of month (01=Jan through 12=Dec)	30
215	D7					36
216	D8				ASCII code, day of month (01-31)	32
217	D9					36
218	DA				ASCII code, vendor specific lot code, may be blank	20
219	DB					20

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
220	DC	7 ~ 4		Reserved		0C
		3		Received power measurements type. 0=OMA 1=Average Power	TRUE	
		2		Transmitter power measurement. 0=Not supported 1=Supported	TRUE	
		1 ~ 0		Reserved		
221	DD	7 ~ 5		Reserved		10 (18)
		4		Initialization Complete Flag implemented. This flag was introduced in rev 2.5. When this bit is 1, the initialization complete flag at byte 6, bit 0 is implemented independent of t_init. When this bit is 0, the initialization complete flag is either not implemented or if implemented has a response time less than t_init, max as specified for the module	Implemented	
		3		Rate Selection Declaration: When this Declaration bit is 0 the free side device does not support rate selection. When this Declaration bit is 1, rate selection is implemented using extended rate selection.	FTLC1151 N/A (FTLC1154 Implemented)	
		2		Application Select Table Declaration: When this Declaration bit is 1, the free side device supports rate selection using application select table mechanism. When this Declaration bit is 0, the free side device does not support application select and Page 01h does not exist		
		1 ~ 0		Reserved		
222	DE			BR Nominal, units of 250 Mbps. Complements Byte 140.	26 Gbps (FTLC1154 28 Gbps)	68 (70)
223	DF			Check code for the Extended ID Fields (bytes 192-222)		68 (98)
224	E0					
225	E1					
226	E2					
227	E3					

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
228	E4			Vendor Specific EEPROM		
229	E5					
230	E6					
231	E7					
232	E8					
233	E9					
234	EA					
235	EB					
236	EC					
237	ED					
238	EE					
239	EF					
240	F0					
241	F1					
242	F2			Vendor Specific EEPROM		
243	F3					
244	F4					
245	F5					
246	F6					
247	F7					
248	F8					
249	F9					
250	FA					
251	FB					
252	FC					
253	FD					
254	FE					

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
255	FF					

ADDRESS A0H PAGE 01 APPLICATION SELECT

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
128	80			CC_APPS:	Check code for the AST: the check code shall be the low order bits of the sum of the contents of all the bytes from byte 129 to byte 255, inclusive.	
129	81	7 ~ 6		Reserved		
		5 ~ 0		AST Table Length, TL (length - 1):	A 6 bit binary number. TL, specifies the offset of the last application table entry defined in bytes 130-255. TL is valid between 0 (1 entry) and 62 (for a total of 63 entries)	
130	82			Application Code 0	Definition of first application supported	
131	83			Application Code 0		
132 ~ 255	84 ~ FF			Application Code TL		

ADDRESS A0H PAGE 02 USER WRITABLE EEPROM

Byte Addr	Hex	LSB	Name	Description	Hex Value
128	80		User EEPROM Data	Customer CLEI code, if page 00h byte 129 is set	
129 ~ 255	81 ~ FF		User EEPROM Data	User EEPROM Data Initialization	

ADDRESS A0H PAGE 03

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
128	80		RO	Temperature High Alarm Threshold MSB	75 deg C	4B
129	81			Temperature High Alarm Threshold LSB		0
130	82		RO	Temperature Low Alarm Threshold MSB	-5 deg C	FB
131	83			Temperature Low Alarm Threshold LSB		0
132	84		RO	Temperature High Warning Threshold MSB	70 deg C	46
133	85			Temperature High Warning Threshold LSB		0
134	86		RO	Temperature Low Warning Threshold MSB	0 deg C	0
135	87			Temperature Low Warning Threshold LSB		0
136	88			Reserved		
137	89			Reserved		
138	8A			Reserved		
139	8B			Reserved		
140	8C			Reserved		
141	8D			Reserved		
142	8E			Reserved		
143	8F			Reserved		
144	90		RO	Vcc High Alarm Threshold MSB	3.63 V	8D
145	91			Vcc High Alarm Threshold LSB		CC
146	92		RO	Vcc Low Alarm Threshold MSB	2.97 V	74
147	93			Vcc Low Alarm Threshold LSB		4
148	94		RO	Vcc High Warning Threshold MSB	3.465 V	87
149	95			Vcc High Warning Threshold LSB		5A
150	96		RO	Vcc Low Warning Threshold MSB	3.135 V	7A
151	97			Vcc Low Warning Threshold LSB		76
152	98			Reserved		
153	99			Reserved		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
154	9A			Reserved		
155	9B			Reserved		
156	9C			Reserved		
157	9D			Reserved		
158	9E			Reserved		
159	9F			Reserved		
160	A0			Vendor Specific		
161	A1			Vendor Specific		
162	A2			Vendor Specific		
163	A3			Vendor Specific		
164	A4			Vendor Specific		
165	A5			Vendor Specific		
166	A6			Vendor Specific		
167	A7			Vendor Specific		
168	A8			Vendor Specific		
169	A9			Vendor Specific		
170	AA			Vendor Specific		
171	AB			Vendor Specific		
172	AC			Vendor Specific		
173	AD			Vendor Specific		
174	AE			Vendor Specific		
175	AF			Vendor Specific		
176	B0		RO	Rx Power High Alarm Threshold MSB	5.50 dBm	8A
177	B1			Rx Power High Alarm Threshold LSB		99
178	B2		RO	Rx Power Low Alarm Threshold MSB	-14.6 dBm	1
179	B3			Rx Power Low Alarm Threshold LSB		5B
180	B4		RO	Rx Power High Warning Threshold MSB	+4.50 dBm	6E
181	B5			Rx Power High Warning Threshold LSB		18

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
182	B6		RO	Rx Power Low Warning Threshold MSB	-10.6 dBm	3
183	B7			Rx Power Low Warning Threshold LSB		67
184	B8		RO	Tx Bias Current High Alarm Threshold MSB	55 mA	6B
185	B9			Tx Bias Current High Alarm Threshold LSB		6C
186	BA		RO	Tx Bias Current Low Alarm Threshold MSB	25 mA	30
187	BB			Tx Bias Current Low Alarm Threshold LSB		D4
188	BC		RO	Tx Bias Current High Warning Threshold MSB	50 mA	61
189	BD			Tx Bias Current High Warning Threshold LSB		A8
190	BE		RO	Tx Bias Current Low Warning Threshold MSB	30 mA	3A
191	BF			Tx Bias Current Low Warning Threshold LSB		98
192	C0		RO	Tx Power High Alarm Threshold MSB	+7.5 dBm	DB
193	C1			Tx Power High Alarm Threshold LSB		AA
194	C2		RO	Tx Power Low Alarm Threshold MSB	-8.30 dBm	05
195	C3			Tx Power Low Alarm Threshold LSB		C7
196	C4		RO	Tx Power High Warning Threshold MSB	+4.5 dBm	6E
197	C5			Tx Power High Warning Threshold LSB		18
198	C6		RO	Tx Power Low Warning Threshold MSB	-4.3 dBm	0E
199	C7			Tx Power Low Warning Threshold LSB		83
200	C8			Reserved		
201	C9			Reserved		
202	CA			Reserved		
203	CB			Reserved		
204	CC			Reserved		
205	CD			Reserved		
206	CE			Reserved		
207	CF			Reserved		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
208	D0			Vendor Specific		
209	D1			Vendor Specific		
210	D2			Vendor Specific		
211	D3			Vendor Specific		
212	D4			Vendor Specific		
213	D5			Vendor Specific		
214	D6			Vendor Specific		
215	D7			Vendor Specific		
216	D8			Vendor Specific		
217	D9			Vendor Specific		
218	DA			Vendor Specific		
219	DB			Vendor Specific		
220	DC			Vendor Specific		
221	DD			Vendor Specific		
222	DE			Vendor Specific		
223	DF			Vendor Specific		
224	E0	7 ~ 4		TX input equalization magnitude identifier. (Controls are found in 234/235)	10 dB (please refer to Table 1 pg 33)	A7
		3 ~ 0		RX output emphasis magnitude identifier. (Controls are found in 236/237)	7 dB (please refer to Table 2 pg 34)	
225	E1	7 ~ 6		Reserved		0F
		5 ~ 4		Rx output emphasis type: '=00 Peak-to-peak amplitude stays constant, or not implemented =01 Steady state amplitude stays constant =10 Average of peak-to-peak and steady state amplitudes stays constant =11 Reserved	0	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		3		RX output amplitude support: Amplitude code 0011 supported	supported	
		2		RX output amplitude support: Amplitude code 0010 supported	supported	
		1		RX output amplitude support: Amplitude code 0001 supported	supported	
		0		RX output amplitude support: Amplitude code 0000 supported	supported	
226	E2		RW	Reserved		
227	E3		RW	Reserved		
228	E4		RW	Reserved		
229	E5		RW	Reserved		
230	E6		RW	Reserved		
231	E7		RW	Reserved		
232	E8		RW	Reserved		
233	E9		RW	Reserved		
234	EA	7 ~ 4	RW	TX1 input equalization control	(please refer to Table 1 pg 33)	1
		3 ~ 0	RW	TX2 input equalization control	(please refer to Table 1 pg 33)	
235	EB	7 ~ 4	RW	TX3 input equalization control	(please refer to Table 1 pg 33)	1
		3 ~ 0	RW	TX4 input equalization control	(please refer to Table 1 pg 33)	
236	EC	7 ~ 4	RW	RX1 output emphasis control	(please refer to Table 2 pg 34)	0
		3 ~ 0	RW	RX2 output emphasis control	(please refer to Table 2 pg 34)	
237	ED	7 ~ 4	RW	RX3 output emphasis control	(please refer to Table 2 pg 34)	0
		3 ~ 0	RW	RX4 output emphasis control	(please refer to Table 2 pg 34)	
238	EE	7 ~ 4	RW	RX1 output amplitude control	(please refer to Table 3 pg 35)	2
		3 ~ 0	RW	RX2 output amplitude control	(please refer to Table 3 pg 35)	
239	EF	7 ~ 4	RW	RX3 output amplitude control	(please refer to Table 3 pg 35)	2
		3 ~ 0	RW	RX4 output amplitude control	(please refer to Table 3 pg 35)	

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
240	F0	7	RW	Rx Squelch Disable Channel 4		00
		6	RW	Rx Squelch Disable Channel 3		
		5	RW	Rx Squelch Disable Channel 2		
		4	RW	Rx Squelch Disable Channel 1		
		3	RW	Tx Squelch Disable Channel 4		
		2	RW	Tx Squelch Disable Channel 3		
		1	RW	Tx Squelch Disable Channel 2		
		0	RW	Tx Squelch Disable Channel 1		
241	F1	7	RW	Rx Output Disable channel 4		00
		6	RW	Rx Output Disable channel 3		
		5	RW	Rx Output Disable channel 2		
		4	RW	Rx Output Disable channel 1		
		3	RW	TX4 adaptive equalization control		
		2	RW	TX3 adaptive equalization control		
		1	RW	TX2 adaptive equalization control		
		0	RW	TX1 adaptive equalization control		
242	F2	7	RW	Masking Bit for high RX Power alarm Channel 1		00
		6	RW	Masking Bit for low RX Power alarm Channel 1		
		5	RW	Masking Bit for high RX Power warning channel 1		
		4	RW	Masking Bit for low RX Power warning channel 1		
		3	RW	Masking Bit for high RX Power alarm channel 2		
		2	RW	Masking Bit for low RX Power alarm channel 2		
		1	RW	Masking Bit for high RX Power warning channel 2		
		0	RW	Masking Bit for low RX Power warning channel 2		
243	F3	7	RW	Masking Bit for high RX Power alarm channel 3		00
		6	RW	Masking Bit for low RX Power alarm channel 3		
		5	RW	Masking Bit for high RX Power warning channel 3		

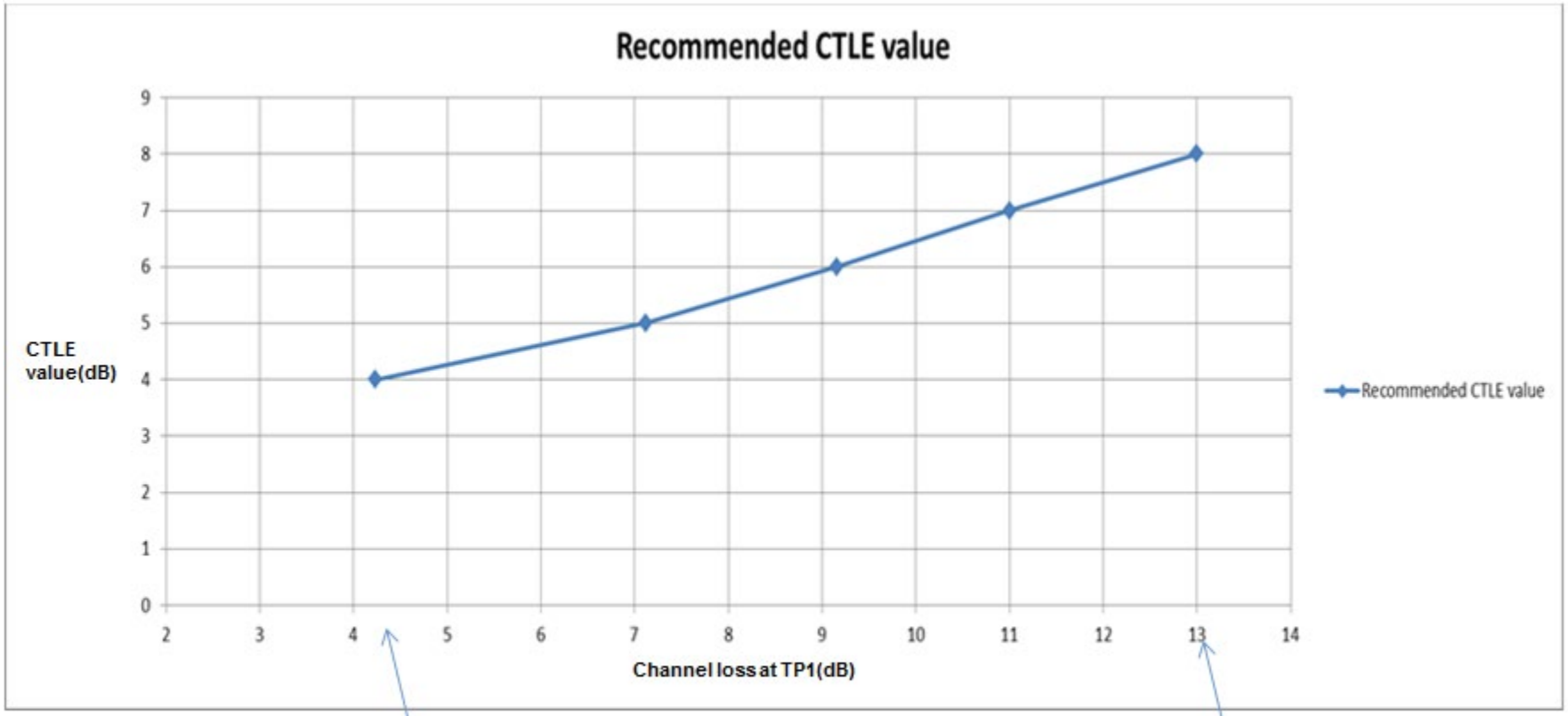
Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		4	RW	Masking Bit for low RX Power warning channel 3		
		3	RW	Masking Bit for high RX Power alarm channel 4		
		2	RW	Masking Bit for low RX Power alarm channel 4		
		1	RW	Masking Bit for high RX Power warning channel 4		
		0	RW	Masking Bit for low RX Power warning channel 4		
244	F4	7	RW	Masking Bit for high TX Bias alarm channel 1		00
		6	RW	Masking Bit for low TX Bias alarm channel 1		
		5	RW	Masking Bit for high TX Bias warning channel 1		
		4	RW	Masking Bit for low TX Bias warning channel 1		
		3	RW	Masking Bit for low TX Bias warning channel 1		
		2	RW	Masking Bit for low TX Bias alarm channel 2		
		1	RW	Masking Bit for high TX Bias warning channel 2		
		0	RW	Masking Bit for low TX Bias warning channel 2		
245	F5	7	RW	Masking Bit for high TX Bias alarm channel 3		00
		6	RW	Masking Bit for low TX Bias alarm channel 3		
		5	RW	Masking Bit for high TX Bias warning channel 3		
		4	RW	Masking Bit for low TX Bias warning channel 3		
		3	RW	Masking Bit for high TX Bias alarm channel 4		
		2	RW	Masking Bit for low TX Bias alarm channel 4		
		1	RW	Masking Bit for high TX Bias warning channel 4		
		0	RW	Masking Bit for low TX Bias warning channel 4		
246	F6	7	RW	Masking Bit for high TX Power alarm channel 1		00
		6	RW	Masking Bit for low TX Power alarm channel 1		
		5	RW	Masking Bit for high TX Power warning channel 1		
		4	RW	Masking Bit for low TX Power warning channel 1		
		3	RW	Masking Bit for high TX Power alarm channel 2		
		2	RW	Masking Bit for low TX Power alarm channel 2		

Byte Address Decimal	Byte HEX	LSB	Type	Name	Description	HEX Value
		1	RW	Masking Bit for high TX Power warning channel 2		
		0	RW	Masking Bit for low TX Power warning channel 2		
247	F7	7	RW	Masking Bit for high TX Power alarm channel 3		00
		6	RW	Masking Bit for low TX Power alarm channel 3		
		5	RW	Masking Bit for high TX Power warning channel 3		
		4	RW	Masking Bit for low TX Power warning channel 3		
		3	RW	Masking Bit for high TX Power alarm channel 4		
		2	RW	Masking Bit for low TX Power alarm channel 4		
		1	RW	Masking Bit for high TX Power warning channel 4		
		0	RW	Masking Bit for low TX Power warning channel 4		
248			RW	Reserved channel monitor masks set 4		00
249			RW	Reserved channel monitor masks set 4		00
250			RW	Reserved channel monitor masks		00
251			RW	Reserved channel monitor masks		00
252			RW	Reserved channel monitor masks		00
253			RW	Reserved channel monitor masks		00
254			RW	Reserved		00
255			RW	Reserved		00

CTLE CHARACTERIZATION

Please see the graph below that shows the CTLE (dB) characterization versus channel loss.

- Please note this is the *recommended CTLE value* for low loss, high loss and channel losses in between.



CTLE CHARACTERIZATION TABLE 1

Default value for CTLE is set to 0x11 for bytes 234 and 235

Channel Loss TP1(dB)	Recommended MSA CTLE (Byte 234&245)
0	0
1	**0**
2	2
3	3
4	4
5	4
6	4
7	5
8	5
9	5
10	6
11	7
12	7
13	8

Rx EMPHASIS CONTROL TABLE 2

We can set the default Rx Emphasis per host recommendation.

Please note the default value for Bytes 236, 237 is 0x00

Total EQ peaking (dB)	MSA Register 236 & 237
0	**0**
0.8	1
1.9	2
2.7	3
4.0	4
5.0	5
6.0	6
7.7	7
Reserved	8

Rx OUTPUT DIFFERENTIAL AMPLITUDE CONTROL TABLE 3

Code	Receiver Output Amplitude (No Output Equalization)	
	Nominal	Units
1xxx	Reserved	mV (p-p)
0111	Reserved	mV (p-p)
0110	Reserved	mV (p-p)
0101	Reserved	mV (p-p)
0100	Reserved	mV (p-p)
0011	600 - 1200	mV (p-p)
0010	**400 - 800**	**mV (p-p)**
0001	300 - 600	mV (p-p)
0000	100 - 400	mV (p-p)

*By default setting for the Rx output amplitude is 0010 (400 – 800mV p-p). This corresponds to MSA Range 2

Parameter	Description	SFF-8679 MSA maximum specification	Measured	Compliant
MSA Table 8-1 timing				
Initialization time t_init	Time from power on *2, hot plug or rising edge of reset until the module is fully functional*3. This time does not apply to non-Power level 0 modules in Low Power State	2000 ms	yes	No. Comply with 4 seconds max
Reset Init Assert Time t_reset_init	A Reset is generated by a low level longer than t_reset_init present on the ResetL input	2 µs	yes	yes
Serial Bus Hardware Ready Time t_serial	Time from power on*2 until the module responds to data transmission over the two wire serial bus	2000 ms	yes	yes
Monitor Data Ready Time t_data	Time from power on*2 to DataNotReady, byte 2, bit 0, deasserted and IntL output asserted	2000 ms	yes	yes
Reset Assert Time t_reset	Time from a rising edge on the ResetL input until the module is fully functional*3.	2000 ms	yes	No. Comply with 4 seconds max
LPMode Assert Time ton_LPMode	Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption reaches Power Level 1.	100 µs	yes	yes

Parameter	Description	SFF-8679 MSA maximum specification	Measured	Compliant
MSA Table 8-1 timing				
LPMode Deassert Time toff_LPMode	Time from deassertion of LPMode (Vin:LPMode =Vil) until module is fully functional*3,*5.	300 ms	yes	No. Comply with 2 seconds max
Software LPMode Deassert Time Byte 93 bit 1 Power_Set is set to 0	Time from deassertion of LPMode (Vin:LPMode =Vil) until module is fully functional*3,*5.	300 ms	yes	No. Comply with 2 seconds max
IntL Assert Time ton_IntL	Time from occurrence of condition triggering IntL until Vout:IntL=Vol	200 ms	yes	yes
IntL Deassert Time toff_IntL	Time from clear on read*4 operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits	500 µs	yes	yes
Rx LOS Assert Time ton_LOS	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted	100 ms	yes	yes
Tx Fault Assert Time ton_Txfault	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted	200 ms	yes	yes
Flag Assert Time ton_flag	Time from condition triggering flag to associated flag bit set (value = 1b) and IntL asserted	200 ms	yes	yes
Mask Assert Time ton_mask	Time from mask bit set (value = 1b)*1 until associated IntL assertion is inhibited	100 ms	yes	yes

Parameter	Description	SFF-8679 MSA maximum specification	Measured	Compliant
MSA Table 8-1 timing				
Mask Deassert Time toff_mask	Time from mask bit cleared (value = 0b)*1 until associated IntL operation resumes	100 ms	yes	yes
Application or Rate Select Change Time t_ratesel	Time from change of state of Application or Rate Select bit*1 until transmitter or receiver bandwidth is in conformance with appropriate specification	100 ms	yes	yes
Power_override or Power_set Assert Time	Time from P_Down bit set (value = 1b)*1 until module power consumption reaches Power Level 1.	100 ms	yes	yes
Power_override or Power_set Deassert Time toff_Pdown	Time from P_Down bit cleared (value = 0b)*1 until module is fully functional	300 ms	yes	yes
*1 Measured from falling clock edge after STOP bit of write transaction				
*2 Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 6.				
*3 Fully functional is defined as IntL asserted due to DataNotReady, bit 0 byte 2, deasserted. The module should also meet optical and electrical specifications				
*4 Measured from falling clock edge after STOP bit of read transaction				
*5 Does not apply to Power Level 1 modules				

Parameter	Description	SFF-8679 MSA maximum specification	Measured	Compliant
MSA Table 8-2 timing				
Rx Squelch Assert Time ton_Rxsq	Time from loss of Rx input signal until the squelched output condition is reached.	80 µs	yes	yes
Rx Squelch Deassert Time toff_Rxsq	Time from resumption of Rx input signals until normal Rx output condition is reached.	80 µs	yes	yes
Tx Squelch Assert Time ton_Txsq	Time from loss of Tx input signal until the squelched output condition is reached.	400 ms	yes	yes
Tx Squelch Deassert Time toff_Txsq	Time from resumption of Tx input signals until normal Rx output condition is reached.	400 ms	yes	yes
Tx Disable Assert Time ton_TxDis	Time from Tx Disable bit set (value = 1b)*1 until optical output falls below 10% of nominal	100 ms	yes	yes
Tx Disable Deassert Time toff_TxDis	Time from Tx Disable bit cleared (value = 0b)*1 until optical output rises above 90% of nominal	400 ms	yes	yes
Rx Output Disable Assert Time ton_RxDis	Time from Rx Output Disable bit set (value = 1b)*1 until Rx output falls below 10% of nominal.	100 ms	yes	yes
Rx Output Disable Deassert Time toff_RxDis	Time from Rx Output Disable bit cleared (value = 0b)*1 until Rx output rises above 90% of nominal	100 ms	yes	yes
Squelch Disable Assert Time ton_sqDIS	This applies to Rx and Tx Squelch and is the time from bit cleared (value =0b)*1 until squelch functionality is enabled	100 ms	yes	yes

Parameter	Description	SFF-8679 MSA maximum specification	Measured	Compliant
MSA Table 8-2 timing				
Squelch Disable Deassert Time toff_RxDis	This applies to Rx and Tx Squelch and is the time from bit set (value =1b)*1 until squelch functionality is disabled	100 ms	yes	yes
*1 Measured from falling clock edge after STOP bit of write transaction.				

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