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Application Note AN-2153

100G QSFP28 LR4 and CWDM4 initialization Application Note Rev B

Introduction

The purpose of this application note is to document the recommended power-on initialization sequence of Finisar's 100 Gigabit Ethernet QSFP28 LR4 and CWDM4 modules. At the time of writing this application note, the affected part numbers are FTLC1151xDPL (25/28G) 10km LR4 and FTLC1152xGPL (25/28G) 2km CWDM4.

The CAUI-4 (4 X 25/28G) high speed signal that propagates from the host ASIC to the module's transmit electrical input can be affected by ISI (inter symbol interference) when the electrical signal is transmitted over long host trace lengths. The accumulation of ISI can distort the high speed signals, sufficient to cause eye closure at the TP1a CAUI-4 input to the QSFP28 module.

Finisar's QSFP28 modules implement a transmit input equalizer function that is designed to compensate the ISI and jitter, to provide an open eye to the transmit CDR (clock and data recovery). Equalization is a signal processing technique that boosts the high frequency component of the signal and reduces ISI. This function is called CTLE (Continuous Time Linear Equalization) and is implemented at the CDR on all 4 input lanes.

Finisar's QSFP28 modules have fixed programmable CTLE implementation.

For more details on the CTLE function please refer to the Appendix on page 5 of this application note.

How to use this Application Note

This application note outlines the default CTLE configuration type in QSFP 28 LR4 and CWDM4 modules and explains how each CTLE method defines the power on sequencing of the module. This will allow the host to determine which CTLE setting best suits their application.

Applicable Documents, Standards and MSA's

a. SFF-8636, QSFP28 100G Common Management Interface Rev 2.6, June 19th 2015.
b. SFF-8679, QSFP28 QSFP28 4X Base Electrical Specification Rev 1.7 August 12th 2014
c. SFF-8024, SFF Committee Cross Reference, Rev 3.5, December 2nd 2015
d. IEEE802.3bm D3p3
e. OIF-CEI-03.1 Common Electrical I/O (CEI) Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O
f. OIF-CEI-28G-VSR Common Electrical Interface - 28G-VSR (CEI-28G-VSR)

Content

The SFF-8636 specifies that the optional equalizer (CTLE) function should be implemented either as fixed programmable or as (automatic) adaptive. Finisar's CTLE mode is fixed programmable, with 1 dB gain. Adaptive CTLE is not implemented.

SFF-8636 Table 6-22 Page 0h, register 193 bit 3 indicates no support for auto adaptive equalizer (set to 0 for unsupported).

SFF-8636 Table 6-22 Page 0h, register 193, bit 2 indicates Manual (*i.e.*, fixed programmable) equalizer support (set to 1 for supported).

The magnitude of the transmitter input equalization supported by the transceiver is identified in Page 03h Byte 224. Here the maximum gain supported is 10dB for fixed programmable mode.

The SFF-8636 Table 6-34 defines the transmitter input equalization in Page 03h bytes 234-235, for the programmable control of the CTLE gain. Please see table below which describes the function of bytes 234 - 235

Byte	Bit	Name	Description	PC	AC	AO	SM
226-233	All	Reserved		-	-	-	-
234	7-4	TX1 input equalization control	Input equalization level control (see Page 03h Byte 224 and Table 6-34)	0	0	0	0
	3-0	TX2 input equalization control	Input equalization level control (see Page 03h Byte 224 and Table 6-34)	0	0	0	0
235	7-4	TX3 input equalization control	Input equalization level control (see Page 03h Byte 224 and Table 6-34)	0	0	0	0
	3-0	TX4 input equalization control	Input equalization level control (see Page 03h Byte 224 and Table 6-34)	0	0	0	0

SFF-8636 Table 6-34 Page 03h Bytes 234-235

	Transmitter Input Equalization	
	Nominal	Units
11xx	Reserved	
1011	Reserved	
1010	10	dB
1001	9	dB
1000	8	dB
0111	7	dB
0110	6	dB
0101	5	dB
0100	4	dB
0011	3	dB
0010	2	dB
0001	**1**	**dB**
0000	0	No Eq

Manual – fixed programmable CTLE

In this method the equalization is fixed for each channel, and the optimum setting can be programmed based on the loss characteristics of the high speed electrical interface. The host has I2C write access to bytes 234-235 and can program the equalization based on the amount of gain needed to correct for the channel impairments. These registers are volatile and so any non-default register value will need to be written upon each module power cycle or reset.

Initialization Process in fixed programmable CTLE mode:

In manual CTLE mode, we recommend that the host follow the initialization sequence described below:

1. Host board is powered on and initialized. The QSFP28 module may or may not already be plugged into the host board. Host should implement low power mode (LPMode pin 31, active High)and hold the module in reset (RESETL pin 9 active low)

2. The host PHY is enabled and configured to the settings that meet the host compliance point TP1.

3. Host brings up the MAC/PCS interface, and CAUI-4 idle packets are transmitted.

4. If not already present in step 1, the QSFP28 module is hot plugged into host.

5. The host releases RESET, and allows 2 seconds for the module to be ready to communicate over the I2C.

6. QSFP28 module is held in Tx disable state by setting Byte 86 to value 0x0F

7. The module ID EEPROM is read and the host configures to the appropriate settings. Host can re-configure the CTLE setting if required.

8. The host releases LPMode pin and releases Tx Disable, the module goes to high power state. Both QSFP28 LR4 and CWDM4 are configured as cooled devices, so the module ready time including TEC stabilization time is a maximum of 5 seconds.

9. Once the optical connections are implemented, the host physical layer link indicator should be asserted.

10. Host will need to read Page 0 byte 2 to clear the latched interrupt state. Interrupt pin 28 will go to high logic state.

11. The MAC/PCS interface can start transmitting data.

Appendix

The IEEE802.3bm D3p3 Annex 83E defines the chip to module CAUI-4 electrical interface.
The CAUI-4 chip to module channel insertion loss is specified to be up to 10 dB at the fundamental frequency of 12.89 GHz.

This allocates 7.3 dB loss for the host, 1.5 dB insertion loss for the module, and up to 1.2 dB electrical connector insertion loss.

The CTLE function defined in section 83E.3.1.6.1 corrects for the unwanted channel loss, present in the host system. This distortion increases with frequency and length of the high speed interface.

The equalizer gain function is given by the following function :

$$H(f) = \frac{GP1P2}{Z1} \times \frac{j2\pi f + Z1}{(j2\pi f + P1)(j2\pi f + P2)}$$

Where $H(f)$ is the CTLE transfer function
G is the CTLE gain
$P1, P2$ are the CTLE poles in Grad/s
$Z1$ is the CTLE zero in Grad/s
j is the square root of -1
f is the frequency in GHz

The graph below represents this function. CTLE gain refers to the relative amount of gain peaking at 12.89 GHz compared to low frequency required to compensate the channel loss over frequency. For example a system that has a short trace length will require a smaller gain setting to correct for the channel imperfections eg 1 dB, whereas a host board that implements a longer trace length between host ASIC to module might require up to 9 dB of amplitude.

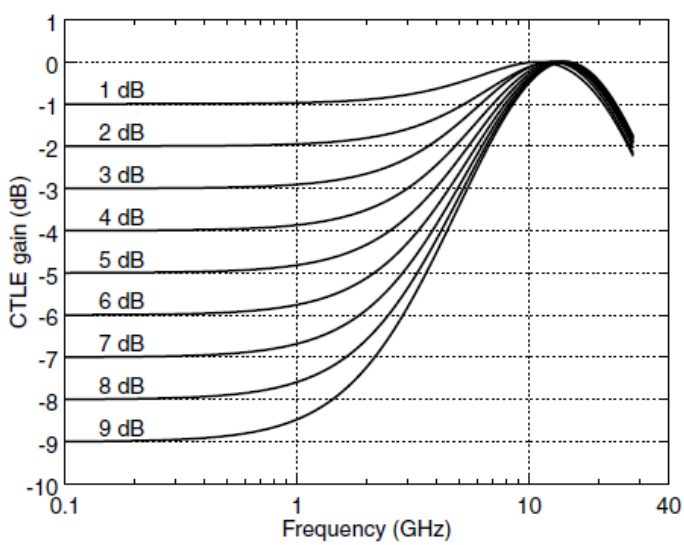

Figure 83E–10—Selectable continuous time linear equalizer (CTLE) characteristic

Finisar QSFP28 transceivers are characterized for CTLE, from IEEE802.3bm D3p3 Figure 83E-9.

Finisar Contact Information

Finisar Corporation
1389 Moffett Park Drive
Sunnyvale, CA 94089-1134
(408) 548-1000
www.finisar.com
sales@finisar.com