Laser material processing in microelectronics manufacturing: status and near-term opportunities
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ABSTRACT
Lasers continue to gain ground in materials processing applications for microelectronics manufacturing. Printed circuit boards, IC wafers, substrates for blue/green LEDs, and various components in flat panel displays are all being processed with lasers. Some of these operations, such as microvia drilling in high-density circuit boards, are well established; others are under evaluation or in early stages of development. This paper summarizes the status of a number of key applications that currently or potentially add value to the complex manufacturing processes for state-of-the-art microelectronic devices. Particular attention is paid to flat panel display manufacturing, where the worldwide mass-production ramp currently underway is demanding innovative techniques that provide the speed, quality, or flexibility needed to reduce manufacturing costs.

Keywords: Lasers, microelectronics manufacturing, semiconductor, flat panel display manufacturing, silicon laser micromachining, laser materials processing

1. INTRODUCTION
Much has been written over the past 40 years about the relentless march of microelectronics technology. Gordon Moore famously observed in 1965 that integrated-circuit technology had until then progressed at a rate that doubled the number of transistors on a single lowest-cost chip every twelve months. This was an empirical assertion initially intended to describe the technology trajectory up until that time, and for the ten years thereafter. In 1975, Moore revised his estimate to slow the density-doubling time to eighteen months, and amazingly, this pace has been kept through at least the early 2000’s. Computing power and memory resources have grown and cost has shrunk exponentially over this period, and while prognosticators continue to forecast the end of Moore’s Law within a technology generation or so, the ongoing advances of solid state scientists and engineers have continued to belie such predictions. More recently, technologists’ consensus seems to be that Moore’s Law will continue to hold for at least another five to eight years, down to the 45nm or 32nm technology node.

We have, for at least a decade, taken for granted the day-to-day gadgets – be they conveniences or necessities – that have come into our lives from this fundamental technology. Here, I mention just three: First, the increases in computing power, speed, and memory resources. Today, one gigabyte of premium Double Data-Rate SDRAM memory can be purchased at any electronics store for about $150, and can be matched with an off-the-shelf CPU operating at 3.0 GHz and costing less than $200. Twelve years ago, when I assembled the first of many PC’s, top-of-the-line processors costing upward of $500 operated at 66 MHz, and 1 Gb of the state-of-the-art slow, “narrow” DRAM memory available to the general public would have cost a whopping $50,000. Such costs (not to mention the manufacturing complexity of high-end components) put the computing power of today’s mainstream laptop computers beyond the realm of all but the supercomputers of 1993. Early 1990’s forecasts of “a supercomputer on every desktop” were prescient: the information-processing world has indeed gotten much, much faster.

Secondly, we consider the proliferation of mobile voice- and data-communication technology. Today, most of the developed world and much of the developing world is covered by mobile cellular telephony infrastructure; if we include satellite telephony, then on-demand linkage between any two points on the planet is within the reach of billions of people. Gone are the days of being out of touch while traveling by foot, bicycle, car, boat, or train; soon airplane travel will be added to this list. Common life activities can be structured differently when instant communication with colleagues, professionals, family, and friends is assured. One result is that the globalization of manufacturing and trade has been accelerated. Today’s global-economy worker can expect to contact or be contacted by colleagues from any time zone on the globe, regardless of his/her location at the office, home, in transit, or while engaged in recreational
activities. Indeed, the availability of on-demand worldwide communication technology has changed our very conceptions of the workplace, as well as the “work pace.” In a word, the world has gotten smaller.

Thirdly, we consider the emergence and growth of the Internet. The look, feel, and common availability of today’s Internet access tools have been with us for only about twelve years. Volumes have been written about the explosive growth and commercialization of the medium that was enabled by the advent of the Hypertext Markup Language and the development of the graphical user interface of modern web browser software. Here, I quote from the online Computer History Museum:

1992: The WWW bursts into the world and the growth of the Internet explodes like a supernova. What had been doubling each year, now doubles in three months. What began as an ARPA experiment has, in the span of just 30 years, become a part of the world’s popular culture.

Arguably more significant, coupled with the massive scale-up of information storage, processing, and retrieval hardware, the ongoing development and commercialization of fast, accurate, and powerful Net search algorithms is enabling a revolution in the way information is obtained, used, synthesized— and indeed in the manner in which learning itself can progress. To cite one small example, the research for this manuscript was done in a manner that would have been impossible ten years ago and only the stuff of science fiction and futurists’ visions fifteen years ago. Shifting between instant, broadband access to the Internet and review and distillation of the information gathered there— all occurring on a computing platform that would have been accessible to only the most rarified strata of the scientific and military establishments twenty years ago, I could pull together a picture of what’s going on in the world of laser microelectronics manufacturing processes in a timeframe that would have been unthinkable then, when I was in graduate school. The Card Catalog is truly obsolete, and the library may not be far behind. In short, the world of the “information consumer” has grown unbelievably richer in the space of a decade.

It is well beyond the scope and intent of this paper to explore the nuances and implications of this faster/smaller/richer revolution in our world, created and fueled by large-scale integrated circuit and ancillary technologies. Yet I believe it is appropriate to step back and acknowledge the profound changes that this technology has wrought in the space of half a lifetime— to point out where it has lead us, how it has shaped our lives. Now, we turn our attention to one part of the “engine” that has created and shaped the technology itself.

2. MICROELECTRONICS MANUFACTURING SEGMENTS

When considering the exponential technology trajectory described by Moore’s Law, it is tempting to focus attention on the devices themselves— to talk about the giant strides in solid-states physics and device technology that have driven the refrain of “smaller, faster, lighter, cheaper” over the past three decades. Yet this is only part of the story. The other part of the picture is the equally impressive innovation that has occurred (indeed, has had to occur), in advanced manufacturing technologies. We recognize the complexity of contemporary semiconductor fabrication processes implicit in the fact that the cost of building a 300-mm fab was over $2 billion in the 2001-2002 timeframe. Recent projections put the cost at more than $10B by 2007.

From the start, the semiconductor industry’s progress was paced by the development of manufacturing technology, not advances in device physics. As Schaller noted in his 1996 paper on Moore’s Law, “It would take advances in technology, specifically process technology, to improve production methods and, in turn, develop a viable semiconductor industry.” Also in 1996, Gordon Moore himself recalled the important role of technology in the early stages: “Indeed, the technology led the science in a sort of inverse linear model.”

Forty years later, the number and complexity of highly sophisticated tools and processes used in the fabrication of today’s chips is remarkable. As a first attempt to classify these tools and processes, semiconductor manufacturing is generally divided into front-end and back-end segments. Loosely speaking, front-end processes include those spanning the creation of the blank silicon wafers through the patterning of the devices residing on each chip. Back-end processes are concerned with test, packaging, and assembly of the finished chips. Lasers play a role in both front-end and back-end semiconductor equipment.

2.1. Laser processes

Figure 1 depicts the “universe” of laser processing in microelectronics manufacturing. In addition to front-end and back-end semiconductor fabrication processes, lasers play a role in two other broad areas of microelectronics
manufacturing: advanced packaging and interconnect (printed circuit boards and chip packages) and flat panel display (FPD) manufacturing. Shown in parentheses are specific processes for which lasers are used in each segment.

**Semiconductor Wafer Processing**  
(Front-end)  
(Lithography, Photomask Mfg., Inspection, Metrology)

**Micromachining**  
(Sapphire, Si, SiC substrates)

**Flat Panel Display**  
(Tilting, ITO patterning, LTPS annealing, Glass cutting)

**Other Markets**  
(Solar cell, Disk drive, Nano-fabrication)

**Semiconductor Test & Assembly**  
(Back-end)  
(Wafer dicing, Marking, DRAM yield improvement, Repair)

**Advanced Packaging & Interconnects**  
(Microvia drilling, Laser Direct Imaging, Flex and Ceramic processing)

Figure 1: The “universe” of microelectronics manufacturing segments and laser-based processes.

Figure 2 presents a collage of commercially available laser-based manufacturing equipment in the four major market segments, giving a snapshot of the range and diversity of tools and processes currently in use. Brief comments about each segment follow.

**Figure 2:** Commercially available laser processing equipment in four major microelectronics manufacturing segments.

### 2.1.1. Semiconductor front-end

As shown in Fig. 2, the laser-based processes associated with front-end semiconductor manufacturing include inspection and metrology—applications where the laser/material interaction yields information about the material, rather than its modification or removal. As such, these applications, while sophisticated and evolving, are outside the scope of this paper.

### 2.1.2. Semiconductor back-end

Back-end laser applications generally involve micro-scale material removal. Some well-known laser materials-processing examples are mentioned here briefly.
2.1.2.1. Trimming
Tuning the value of discrete electronics components (resistors, capacitors, inductors) or the response of entire circuits is a well-established laser process, dating back some thirty-five years. The technology is mature, and while there has been some interest in shorter wavelengths to improve resolution or stability of the treated components, most innovation in recent years has focused on integration of high-speed, real-time measurement of component or circuit characteristics for closed-loop control of the tuning process. Extension of the technique from thick-film to thin-film components and circuits has also been an area of progress.

2.1.2.2. Memory Yield Improvement
Yield improvement of DRAM memory chips gains its name from the significant increase in overall yield it provides, particularly for high-end (dense) chips. After testing of the memory cells on each chip is conducted, single laser pulses sever individual “links” in the chip circuitry, thereby isolating defective cells and bringing online spare cells built into every chip. Many more chips are thereby brought up to the design specifications for memory capacity. State of the art systems focus the laser spot to slightly over 1 µm in diameter, position it with sub-micron accuracy, and process upwards of 30,000 links per second. Recent advances have pushed laser wavelengths into the UV, in order to decrease focused spot size further to follow industry process shrinks below the 90nm node and to optimize laser interactions with newer materials such as copper and low-k dielectrics.

2.1.2.3. Wafer marking
Laser wafer marking has been used for more than 20 years due to its high speed, inherent flexibility (marks are easily and rapidly tailored) and the need to pack progressively more manufacturing-process traceability information into the marks. Marks are typically generated by 1064-nm Nd:YAG lasers and are classified as either “hard” (60-80 µm depth) or “soft” (< 5 µm). Hard marks are produced outside the cleanroom and due to their greater disturbance of the silicon substrate, are suitable for only marking only the wafer backside. Soft marks are generated in the cleanroom and are suitable for both backside and topside (active side) marking of chips. Some innovations driven by the need for Marks that do little or no actual removal of material, leave zero ridge height surrounding each mark site, and/or minimize or eliminate heat-affected areas near the mark have recently been reported.

2.1.2.4. Wafer Dicing
Finally, laser dicing and scribing of wafers has received much attention in the past four to five years. This application is one of the “near-term opportunities” discussed in detail later in this paper.

2.1.3. Advanced packaging
In the Advanced Packaging and Interconnect segment, two specialized laser processes have enjoyed successful commercialization in recent years: Microvia drilling and Laser Direct Imaging (LDI).

2.1.3.1. Microvia drilling
During the last seven to eight years, much attention has been focused on the development and evolution of laser microvia drilling in the Printed Circuit Board (PCB) and chip packaging segments. Driven in the PCB world by the migration to so-called High Density Interconnect (HDI) design rules for consumer-electronics products such as cell phones, the technology won out over several competing techniques in the late 1990s as via-hole diameters dropped to 150 µm and below and conventional mechanical drills became non-cost-effective. Laser drilling has been scaled up to higher and higher throughputs through the use of more powerful lasers operating at higher pulse repetition rates; faster galvanometer-based beam positioners; and the introduction of modest amounts of parallelism (multiple beams) into advanced equipment.

CO₂ lasers continue to dominate for HDI applications, since the minimum via diameter of about 75 µm needed for HDI circuits boards is within the capabilities of the 9-10 µm wavelength. Multi-layer substrates common in the so-called Chip-Scale Package (CSP) segment, however, often feature circuit layouts that require vias of 50 µm and smaller diameter. For these advanced chip packages, UV diode-pumped solid state (DPSS) lasers— typically third harmonic
Nd:YAG or Nd:Vanadate lasers at 355 nm wavelength—have gained acceptance as the technology of choice. Efforts over the last several years have focused primarily on parallelism and cost-reduction in the drilling tools.

2.1.3.2. Laser Direct Imaging (LDI)

This process has enjoyed a resurgence in the PCB manufacturing segment in the past two years. The driver for this renewed interest has been the increasing need for better “true positioning” of small features on large PCB substrates, to compensate for inevitable layer-to-layer mis-registration and material distortion imparted during the lamination process. Current LDI tools embody a third generation of the technology, the first of which dates back to the id 1980s; both prior generations failed to take hold in high-volume manufacturing because the technology was not greatly better and certainly no less expensive than conventional patterning techniques. Technical issues with the laser sources and available photoresists also hampered previous-generation adoption.

In the LDI technique, a cw or quasi-cw UV or violet laser replaces the broadband light sources (arc lamps) traditionally used to expose thin photoresist layers laid atop the PCB substrates. Rather than conventional photolithography, where the patterns in the resist are obtained by exposing it to an image projected through a mask, the laser beam impinges directly on the areas of the resist that are to be cross-linked.

The photolithographic process being replaced by LDI achieves exposure of the entire large PCB substrate at once, whereas the most common implementation of the LDI process is inherently serial, with the laser beam exposing only small spots at any time. LDI spot sizes must be kept small in order to keep the “pixel” (smallest exposed feature) size comparable to or better (smaller) than that obtained with lithography—which today is about 75 µm for most PCB shops. As a result, the small focused laser spot must be moved over the substrate at extremely high speed in order to achieve satisfactory process throughput and cost-effectiveness.

Modern systems have migrated away from cw ion lasers to quasi-cw modelocked third-harmonic DPSS lasers, due to better stability and reliability. The beam is scanned in a high-speed raster pattern, using a rotating polygon mirror and precision large stages. Pixels are selected for exposure by high-speed modulation of the laser beam, typically with acousto-optic devices. An alternative technology sequentially images small portions of the substrate, spatially modulating the laser light over this small area with devices such as Texas Instruments’ Digital Mirror Device. The “working area” is stepped across the substrate to achieve large-area coverage.

LDI systems are complex and expensive. They have gained acceptance in both high-end PCB applications (which may require the smaller circuit lines and spaces achievable with the technology) and in shops that do rapid-turnaround low-volume runs of prototype or custom boards. In the latter case, the cost of creating new phototools (masks) for each new PCB layout becomes great enough to make the initial large capital investment in an LDI system an economically attractive alternative.

As feature sizes are driven downward in future-generation electronics products, layer-to-layer alignment tolerances will become tighter and layer-by-layer compensation for distortion—which cannot be achieved with conventional phototools—will become increasingly critical. These technology drivers should make LDI an increasingly compelling capability for mainstream PCB manufacturing shops.

2.1.4. Flat Panel Display

This microelectronics segment has experienced explosive growth over the past five years. Several laser processes are well established in FPD manufacturing, while a number of others are emerging as near-term opportunities. Due to the dynamic nature of this industry and the increasing pressure to bring manufacturing costs down, we believe that FPD manufacturing is a fertile area for new laser materials-processing processes, and so devote a separate section to it later in the paper.

2.2. General observations on manufacturing technology adoption

Most of the laser materials-processing applications cited above have undergone continuous changes and improvements over the last five to ten years. However, once past the early days of technical feasibility demonstration and early adoption in high-end niches where their use is a necessity, technical performance is not the determinant of their continued success. Rather, their comparative cost-effectiveness is what is key.
In the early days of a manufacturing technology’s adoption, it typically must enable some aspect of the process: laser drilling enabled the incorporation of microvias into common PCB products, while early link-processing enabled the primary manufacturing yield of 16 Mb DRAM chips to climb out of single-digit values. Later in the technology maturation process, however, cost becomes the driving factor. Continued technology improvements, while perhaps directly related to process speed, are motivated by the need to decrease cost per unit throughput. Process robustness, tool reliability, speed and precision can all play a role in ongoing technology innovation, but the driver is cost. And in recent years, the pace of the transition from performance-as-driver to cost-as-driver has accelerated.

This is a direct result of the increasing complexity of the equipment needed to fabricate ever-smaller devices with ever-larger scales of integration. For example, today new technologies are being vigorously pursued to develop so-called Extreme UV light sources with 13nm wavelength, to enable optical lithography techniques to be extended to the 30nm node and beyond. But if these light sources cost on the order of $10 million, as some projections estimate, then even if they are enabling for the 30nm technology node, the sheer capital cost of a litho tool could sink the technology. This, then, is an example of cost considerations entering at the very beginning of a technology’s maturation cycle: in the near future, it will no longer be sufficient for a new technology to enable next-generation manufacturing capabilities, if the “cost-of-ownership” calculus is unfavorable.

Such considerations are worth bearing in mind as we evaluate the drivers, performance, and alternative techniques for candidate near-term laser materials-processing opportunities in microelectronics manufacturing in the next section. Without such cost-related constraints, the mid-1990’s comments of Dan Hutcheson, President of VLSI Research, could well come true:

“Moore's Law will fall victim to economics before it reaches whatever limitations exist in physics.”

3. NEAR-TERM OPPORTUNITIES FOR LASER PROCESSES

3.1. Silicon Micromachining

Silicon has for a number of years been a prime material candidate for laser micromachining applications, particularly since the late-1990’s introduction of reliable UV DPSS lasers. Laser-ablative fabrication techniques for MEMS, MOEMS and other micro-scale devices have been explored at the feasibility level, but the widespread availability and maturity of semiconductor Si micromachining technology has generally been a formidable obstacle to mass-production scale-up. Compounding this effect is the fact that the smallest length scales at which lasers can effectively remove material (not far below 1 μm) do not represent leading-edge processes for semiconductor fabrication. So any Si device design that might lend itself to laser micromachining would typically require only earlier-generation semi fab equipment, which is relatively cheap and accessible. A clear exception to this is high-aspect-ratio 3D micromachining, but so far the need for this has been quite limited.

The barriers to large-scale commercialization of laser Si machining are changing, however, and the driver has less to do with the emergence of new Si devices than new problems with old ones.

3.1.1. Thin wafer dicing

After the devices are fabricated on its individual chips, a semiconductor wafer is traditionally cut apart or diced by an automated precision mechanical saw. The technology has existed since the early days of the industry and is quite mature, with complex saw blade designs and process recipes. Though it is a wet process, mechanical wafer dicing has been widely accepted for decades. So why replace it with a laser?

If the answer were only “because the laser dicing process has no consumables (saw blades) to wear out and need routine replacement,” this would not be enough to justify a technology shift to lasers. Other possible reasons include the following:

- The process is “dry,” in contrast to the mechanical sawing process.
- The laser can create a smaller cut width or kerf. This enables the streets between neighboring dice on the wafer to be narrower, allowing more chips to be packed onto a given wafer size (e.g. 200 mm).
Unlike mechanical sawing, laser cutting is not confined to straight lines. Curvilinear shapes such as the outlines of Arrayed Waveguide Gratings can be excised.

Different die sizes and shapes can be “nested” on a single wafer, permitting more efficient use of the available silicon real estate.

While all of the above are true, none of these “benefits” of laser dicing, either individually or taken collectively, offer sufficient motivation to abandon the conventional saw technology. As usual, cost is the primary true driver here, rather than enhanced capabilities—but only for a portion of the overall wafer-dicing market. Laser dicing is much slower and therefore more expensive for most of today’s wafers.

The real motivation is that the laser technology is more cost-effective for one of the directions that the industry is moving: to thinner wafers. Two market forces are driving the move toward thinner wafers. First, new applications such as embedding memory or logic chips in very thin devices such as “smartcards” require thin chips. Today, this is a niche market and a large growth rate, while anticipated, is not certain.

Second, and more compelling, today’s portable consumer devices must carry substantial amounts of onboard memory to provide the feature-rich operations we have come to expect and demand. Given the small footprint of these devices, advanced chip packagers are turning more and more toward 3D strategies involving stacking of dice. Figure 3 shows SEM micrographs of several versions of four-die stacks. The package in Fig. 3b is composed of four die with two spacers; the 200-mm wafer used here is thinned down to 75 µm. Figure 4 shows a 3D-packaging “roadmap,” depicting the thickness to which individual die must be ground to achieve desired total package heights, for the stacks of up to seven dice currently in development.

The drive to pack more functionality into the small footprint required by handheld electronic products, and at the same time to reduce packaging costs, is a powerful market force pushing the industry toward thinner and thinner wafers. Not only can stacked-die packaging meet the footprint constraints of these products, but it also provides a cost-reduction benefit. With regard to a four-die package introduced by ChipPAC in 2003, the company reported that “The package cost, driven by the use of only one package substrate for all chips, is about 40 percent less than the total cost of individually packaging four chips.” The company’s COO concluded at that time:

“We have made [stacking of chips] a core competency of our company and it is targeted at the fastest growing areas of electronic product demand. We should continue to see strong growth in these areas for years to come.”

So why is this good news for laser dicing? Though mechanical sawing technology continues to progress, the technology starts to encounter difficulties as wafer thickness drops below about 100 µm. To avoid backside chipping (Fig. 5), the saw feed speed must slow dramatically and/or the saw must resort to multi-pass process recipes. At the same time, as wafer thickness decreases, the through-cutting speed achievable with lasers increases—and does so non-linearly. As a result, there is a crossover point in the dicing speed (and hence cost) of mechanical and laser technology. Current power levels of DPSS 355-nm wavelength lasers (~10 Watts) put this crossover thickness at between 125 and 150 µm. For wafers thinner than this, the laser process is faster (Fig. 6).
Die thickness

Package height (mm)

Figure 4: Stacked-die packaging roadmap. All stacked-die packages require wafer thickness of less than 125 µm. As of mid-2003, packages with up to five stacked chips were reportedly in high-volume production.\(^{15}\)

As both laser and chip-packaging technologies progress, laser power will continue to increase and wafer thickness to decrease. Consequently, there will be a natural shift of the wafer thickness at which laser dicing becomes more cost-effective than mechanical sawing, toward higher values. This is depicted schematically in Fig. 6. Even as the industry drives toward thin wafers for 3D packaging needs, continued progress in laser power scaling will open up more of the total wafer dicing market to the laser process. This is the basis of our belief that silicon wafer dicing is an emerging high-volume application for laser processing.

3.1.2. Low-k layer scribing

As semiconductor device dimensions shrink according to the industry roadmap, operation speed is determined by signal propagation times along “global” interconnects linking widely separated on-chip devices. The propagation delay of these interconnects is governed by both the resistance of the conducting pathways and the wiring capacitance (RC delay). Substitution of copper for aluminum conductors circa 1997 addressed the former of these; the latter is determined both by cross-sectional size (and hence spacing) of the interconnect wires and the permittivity or dielectric constant, \( k \), of the inter-level dielectric (ILD) material surrounding the wires.

Starting at about the 180-nm generation, wiring density became sufficiently high that copper alone would not address the unacceptably high RC propagation delays; lowering the dielectric constant of the ILD was also clearly needed. This is the reason why low-k materials have been the focus of intensive research in the past ten years: they enable chipmakers to build chips with Cu interconnects having acceptably low wiring capacitance. Low capacitance permits high-frequency signals to move between devices with low RC propagation delay, even as device size continues to shrink and wiring density grows. That’s why low-k dielectric is essential to building current and future chips: it is an enabling technology.

Figure 7 shows the construction of the on-silicon interconnect layers with low-k ILD material. Low-k materials continue to evolve: though all chips fabricated at the 90nm node and below will have low-k ILD, the material is substantially different from the low-k dielectric first used at the 180 and 150 nm nodes\(^{14}\). While the latter was a fluorinated version of the SiO\(_2\) glass used as ILD since the dawn of the industry, the newer low-k materials are complex organic or inorganic materials; organo-silicates; and other, hybrid formulations.
More important for discussion here, one pathway to low dielectric constant is to introduce porosity into the material. This approach has been intensively explored and put into commercial chips beginning with the 90nm node in 2004. Unfortunately, these porous low-k dielectrics have significantly poorer mechanical strength than conventional SiO$_2$, and dicing with saws becomes problematic. In particular, the blade wreaks havoc with metal test structures commonly placed in the streets between die, resulting in extensive chipping and/or delamination of the Cu/low-k stack from the underlying silicon substrate (Fig. 8). To date, it has been impossible to completely eliminate this issue with dicing saws. The result is a yield hit for high-value chips such as central processing units or graphics processing units.

A potential solution that has received much attention is to combine laser scribing of the low-k stack with subsequent through-dicing of the Si substrate by conventional diamond saw blade. Figure 9 illustrates the concept and results. Research and development on this approach, on laser-only approaches, and on an innovative laser/waterjet hybrid technique are currently active areas of investigation.

Figure 7: Copper/low-k interconnect architecture. (a) schematic showing four metal layers and porous low-k ILD. (b) cross section of Intel 7-layer interconnect structure used on 90nm processor chips.

Figure 8: Chipping and de-lamination of low-k layers caused by diamond dicing-saw blade.

Figure 9: Two approaches for combined laser-saw dicing of low-k wafers. In (a), two grooves are made in the low-k layer with the laser, close to the edges of the street. Cracks created by subsequent sawing through the center of the street are stopped by the laser scribe lines. In (b), a single, wide laser trench is created in the center of the street prior to sawing. Removing the low-k material in the path of the saw helps reduce loading of the blade with the soft dielectric. (c) Example of the two-groove scheme.
3.2. Flat Panel Display Manufacturing

This segment of the microelectronics industry has experienced enormous growth in the last five years (Fig. 10), with a recent forecast putting the Compound Annual Growth Rate (CAGR) at 26% for the period 2002-2006. Currently, televisions and desktop monitors dominate revenues, with TV’s expected to surpass monitors in 2007. Of the technologies used to produce FPDs, Active Matrix Liquid Crystal Displays (AM-LCDs), also known as Thin-Film Transistor LCDs (TFT-LCDs), dominate the field, with over 80% market share beginning in 2004 (Fig. 10b).

![Figure 10: Revenue growth of flat panel display market. (a) by application, including LCD, PDP, and OLED devices. (b) by technology, showing dominance of TFT-LCD.](image)

As the FPD industry has evolved, several trends have emerged. The main technical driver for successive manufacturing generations is the size of the glass substrate upon which the displays are built. Larger substrates drive economies of scale, so each new generation represents a significant areal increase over the previous one. Due primarily to the growing substrate size and the increasing complexity of manufacturing equipment, FPD fab capital costs, like semiconductor fab costs, have skyrocketed. Also similar to the semiconductor industry, fewer companies, as a result, have been able to afford to build fabs with each successive generation. These trends are summarized in Figure 11 for the LCD segment.

Despite the escalating costs of building FPD fabrication plants, the selling price of finished displays has experienced tremendous downward pressure over the past several years, and this will continue. DisplaySearch reports that FPD average selling prices (ASPs) for the 14”, 19”-21”, and 28”-32” size segments will be –10%, -15%, and –19%, respectively, for the period 1998-2006.

The combination of high revenue growth rates, exponentially increasing capital costs, and decreasing ASPs lends significant motivation to the ongoing drive to reduce manufacturing costs. For this reason, if no other, we believe that the FPD manufacturing industry is fertile ground for innovative laser-based processes—if they are either enabling (as substrates grow larger and increasing levels of on-glass component integration emerge), or they offer substantial costs-savings over previous-generation technology. The following sections focus attention upon TFT-LCD technology and current and emerging laser-based manufacturing processes in this segment.

![Figure 11: LCD manufacturing industry dynamics: growing substrates, rising fab costs, fewer players. (Sources: DisplaySearch, Fuji Chimera, iSuppli, & US Display Consortium) Adapted from Ref. 19.](image)
3.2.1. Overview of TFT-LCD devices

Before discussing specific laser-based manufacturing processes, we briefly review the construction and functioning of a TFT-LCD display. The basic elements of such a display are shown schematically in Figure 12. White light from a broadband source (typically one or more fluorescent tubes) is dispersed by a Light Guide Panel (LGP) and passes through a polarizing filter. It then enters the TFT array, which is the heart of the device. Here, a matrix of many thin-film transistors functions as an array of switches, each providing a switchable, localized electric field that influences the behavior of the thin layer of liquid crystal (LC) material in the adjacent LC cell.

The LC material performs the function of spatial light modulation, due to the orientation of the LC molecules relative to the narrow dimension of the LC cell. Each “subpixel” of LC material can either block or pass the incident light, depending on the presence or absence of the field generated by the TFTs. Atop the LC cell and carefully aligned with it and the TFT array, a color filter creates the red, green, blue primary colors from the incident white light, combining groups of individually-colored sub-pixels (each controlled by a separate TFT) into each display pixel. The display is viewed through a top layer of polarizing film.

Figure 12: Schematic view of a TFT-LCD panel. Variations in construction are many, but the most common design places the TFT array and color filter on separate glass substrates, with the liquid crystal material sandwiched between them in a thin layer.

Figure 13 shows a cross-sectional view of an assembled TFT-LCD panel, with current and emerging laser processes highlighted for the affected components. In the next sections, we discuss these individual processes.

Figure 13: Cross sectional view of a TFT-LCD panel, showing current and emerging laser applications.
3.2.2. TFT annealing

The TFT annealing process, typically accomplished with XeCl excimer lasers, was commercialized in the late 1990s. The laser is used to induce localized melting and re-crystallization of a thin layer of amorphous silicon (a-Si) previously deposited on the glass substrate. The rapid heating and cooling rates generated by the laser transform the a-Si to a polycrystalline phase (p-Si); i.e., individual crystal grains separated by grain boundaries. Because the bulk substrate remains cool, the process (and the technology) is commonly referred to as Low Temperature Poly Silicon (LTPS). An excellent review of various polysilicon crystallization schemes is given in Ref. 20.

The task of transforming the a-Si layer to p-Si is motivated by the desire to improve the field-effect mobility in the TFTs, thereby reducing their switching time. This faster response is not necessary for the basic TFT array circuitry, however, and for that reason, most of today’s TFT-LCD displays do not use LTPS: only about 10% of total LCD fab capacity was devoted to LTPS production in 2004.

Indeed, the motivation for employing LTPS is not to increase the dynamic response of the display pixels, as the low intrinsic mobility of a-Si (< 1.0 cm²/V-s) is acceptable for pixel-switching speeds. Rather, the higher mobility of LTPS (50-150 cm²/V-s) opens the door to fabricating higher-speed driver circuitry directly on the glass substrate (around the periphery of the display array). In the future, even higher mobilities will enable even higher levels of system integration. The ability to eliminate separate driver ICs (see Fig. 13) and the bulky and expensive flexible circuits wiring them to the signal lines on the glass can save cost and is of significant value in the world of handheld electronic products, where compactness is critical.

3.2.2.1. Excimer laser annealing

Conventional excimer-laser annealing (ELA) employs lasers with average power between 200 and 1000 W, forming the beam into a line that is scanned across the substrate surface. Line length and irradiance-profile uniformity are key factors in process speed and quality, respectively. The process yields small grains, typical around 0.3 µm. Because field effect mobility depends on grain size (Fig. 14a), grains larger than this are desirable. The grain size, however, depends sensitively on the physics of the melting and re-crystallization process: ideally, the process would achieve complete melting through the entire thickness of the a-Si layer, since this produces the largest grains (Fig. 14b). However, running the annealing process at this condition (near the peak of the curve in Fig. 14b) leads to problems. Because the melt dynamics are critically sensitive to the laser fluence applied to the layer, relatively small fluctuations in laser pulse energy (~ 5%) lead to large variations in grain size. Over a large substrate, therefore, unacceptable variations in TFT device performance can occur if the ELA process is run in the “full melt” regime. Consequently, the process is run in the “partial melt” regime, producing relatively small grains.

![Grain Size vs Laser Energy Density](image)

(a) Field Effect Mobility vs. Grain Size

(b) Grain Size (µm)

Figure 14: Details of mobility, grain size, and laser fluence in the ELA process. (a) Field effect mobility scales with size of the p-Si grains. (b) Grain size depends sensitively on laser fluence. Consequently, the ELA process must be run in the partial melt regime, yielding relatively small grains.

3.2.2.2. Sequential Lateral solidification

Due the inherent grain-size limitations of ELA, numerous variations of the annealing process have been explored. In the late 1990s, James Im and his group at Columbia University developed a promising technique called Sequential Lateral Solidification (SLS). Samsung commercialized the process in 2002. SLS uses the same excimer laser as ELA,
but the beam is passed through a mask and imaged onto the substrate with precision projection optics. The beam is split by the mask-projection technique into multiple small beam lines, spaced a precise distance apart. Each beamlet melts a stripe of the a-Si layer about 6 µm wide. Upon cooling, re-crystallization proceeds laterally, inward from the edges of the stripe toward its center. Full melt can be achieved, thereby producing larger, elongated grains, while eliminating the sensitivity of the ELA process: the SLS process tolerates laser energy fluctuations up to about 30%. Figure 15 shows a comparison of grain sizes and mobility values produced by ELA and SLS.

Along with the larger grains and higher mobilities, SLS provides another benefit compared to ELA. Because (in its most common variation) SLS requires only two laser shots per location compared to about 20 for ELA, it is faster. For substrates measuring 30 x 470 mm, an SLS cycle time of 58 s is reported; the comparable ELA process cycle time is 78 s. A disadvantage of SLS, however, is its very short depth of focus: about 30 µm compared to ~300 µm for ELA. This imposes tighter constraints on the annealing system’s opto-mechanics, leading to somewhat higher system cost.

### 3.2.2.3. DPSS laser annealing

Research in laser annealing for LTPS is currently quite active. The reason is that mobilities even higher than the 300 cm²/V-s achievable by SLS will be needed for even higher levels of system integration. Beyond the second-generation LTPS products which feature integrated driver circuitry, the third generation will integrate all or most of the entire computational logical and memory subsystems. Such so-called “System on Glass” architectures will require mobilities of > 500 cm²/V-s, approaching that of single-crystal Si. Recent research has shown that grain sizes substantially larger than 10 µm can be achieved with both pulsed and cw DPSS neodymium-based lasers operating at the second harmonic (532 nm wavelength). Commercialization of the technology will be paced by availability of such green-wavelength lasers with average output powers of 200-300 W.

### 3.2.3. ITO patterning

All FPD architectures use thin films of transparent, conductive indium tin oxide (ITO). In LCD panels, ITO circuit traces route signals to the TFT array and ITO forms the TFT electrodes; in plasma display panels (PDPs), the discharge electrodes that generate the plasma are ITO. The conventional means of patterning the ITO layer is photolithography. For very large substrates, however, lithography becomes prohibitively expensive and technically problematic. Direct laser patterning of the ITO layer is emerging as an alternative. The laser process may represent enabling and/or cost-saving technology. Laser patterning can be of two general types: direct ablation and resist exposure.

#### 3.2.3.1. Direct ablation

In laser direct ablation, a high-power multimode 1064 nm-wavelength laser is used to directly remove the ITO layer. Exitech (Oxford, UK) has developed a prototype system, shown schematically in Fig. 16. Since the process is inherently serial, throughput is a key issue and therefore the system is designed for scalability. Multiple galvo-scanning heads are individually fed by remotely located fiber-coupled lasers, each emitting >100 W. To minimize risk of substrate damage due to hot spots, the beam for each laser+scan head unit is transformed to a uniform irradiance profile. Mask imaging shapes the laser spot to match the desired shape of the ITO pattern (Fig. 17). Tool design issues include effective debris handling, achieving beam placement accuracy of ~10 µm over large display panels (up to > 60”), and maintaining the laser spot within a short focal depth over large areas.
3.2.3.2. Resist exposure

In this approach, which is less developed than the direct-ablation scheme, the laser is used to exposure the photoresist. The exposure step is followed by conventional develop, etch, and resist-stripping steps. The concept is similar to LDI, and a 355-nm quasi-cw DPSS laser is the exposure tool of choice.

3.2.4. Other laser-based FPD manufacturing processes

3.2.4.1. Glass separation

This laser process is vying to replace conventional diamond-wheel scribing for excising FPD panels from the large substrates. The process is based on controlled crack propagation. After a crack is initiated mechanically or with another laser, a CO$_2$ laser is used in tandem with a gas or liquid jet to rapidly heat and cool the glass. Thermally-induced stresses propagate the crack vertically into the substrate and in the direction of beam motion, as the beam is traversed along the separation line.

In one variation of the technique, a second CO$_2$ laser follows the cooling jet in order to propagate the crack vertically all the way through the glass, so that no further operations are required. When the process is properly controlled, the separation edge can be atomically smooth, with no chipping, melting, or other distortion. Breaking the glass along scribe lines and post-break edge grinding to remove cracks are eliminated, thereby reducing process cycle time as compared to diamond-wheel scribing. Because capital costs for laser separation tools are substantially greater than abrasive-wheel systems, adoption of this technology into high-volume production has been relatively slow.

3.2.4.2. Titling

Low-power UV DPSS lasers are being used in production to mark brand or production-traceability information into FPD glass substrates. The most common wavelength is 355nm, since it permits intra-glass marking via controlled, localized microcracking inside the bulk material, and therefore generates zero debris.

3.2.4.3. Light guide panel engraving

The acrylic plastic diffuser or light guide panels (LGPs) that guide and disperse the white-light illumination for LCD panels are created by controlled engraving. Patterns embossed in the surface of the transparent material function as scattering centers, re-directing and homogenizing light propagating sideways through the plastic so that it propagates in a direction normal to the embossed surface. The conventional technology is mechanical stamping, which is far less expensive than the laser process. However, light scattering from laser-engraved patterns has been found to be more efficient than that of the embossed patterns, permitting one diffusing surface to be used rather than two. Cost reduction of the finished assembly is thus the motivation for adoption of the laser process, which is pending process refinement.
4. SUMMARY

Laser processing is alive and well in the various microelectronics manufacturing industries. Silicon micromachining for wafer dicing will likely achieve mass production due to cost-saving and enabling aspects of the technology, and the sheer volume of the industry. FPD manufacturing will continue to see vigorous growth, and the laser-processing opportunities are many. To provide today’s sophisticated microelectronics products at the prices we consumers expect, developing sophisticated but cost-effective manufacturing technologies is critical. Processes that survive the road to commercial mass production will of necessity be cost-effective, reliable, and better than non-laser alternatives. It’s a “Darwinian” selection process: only the economically “strongest” processes survive.

ACKNOWLEDGEMENTS

The author thanks the following people for contributing material or discussion to the preparation of this paper: Jim Fieret (Exitech); Jan Bruner (MicroLas/Lambda Physik); Dick Toftness (Xsil); Brian Hoekstra (Applied Photonics); Sri Venkat (Coherent); David Clark (Coherent); Stephen Lee (Coherent).

REFERENCES

10. See, for example, Disco corporation: www.disco.co.jp